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Design and Study the Performance of a CMOS-Based Ring Oscillator Architecture for 5G Mobile Communication

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Abstract

Oscillator circuits are used to make accurate and reliable clock signals for systems as simple as a wristwatch and as complicated as satellites, which are important for long-distance communication. There are many ways to build an oscillator circuit, using either passive or active parts. Each option has pros and cons, but at the current level of mobile communication development, the most important things are interoperability and low power use. This need has driven the development of compact, battery-operated electronics, and Very Large-Scale Integration (VLSI)-based ring oscillators provide the ideal solution. These oscillators ought to dissipate less power, have a large tuning range, and be compact. The paper presents a novel Complementary Metal Oxide Silicon (CMOS) ring oscillator that serves as a Voltage Controlled Oscillator. The suggested architecture utilizes the advantages of both a current-starved ring oscillator and a negative-skewed delay by combining their constituent parts. The proposed architecture has a control voltage of 1.15 V and a supply voltage of 2 V, generating a 9.35 GHz dominant frequency with a 13.82% harmonic distortion between the inputs and outputs. The proposed architecture can implement 5G-based applications that require high frequency and low power by carefully selecting the passive components within the design.

Keywords:

VLSI; 5G;
CMOS; Ring Oscillator;
VCO;
Mobile Communication.

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1- Introduction

RF circuits typically employ radio signal transmission frequencies; therefore, they are considered high-frequency circuits when compared to analogue circuits, which are considered low-frequency. Methods of frequency domain analysis, such as Fast Fourier transformations, are utilized in the analysis of RF circuits. This enables RF designers to model circuits based on harmonic and carrier frequencies. In addition, frequency domain analysis provides information on frequency-dependent parameters, such as noise, interference, and general waveform accuracy. Engineers conduct numerous analyses based on the problems they encounter during the RF design procedure. Oscillators are an essential component of every communication system. The primary mechanism for generating a clock signal is through oscillators. All electrical circuits rely on a clock signal to control their operation and keep track of processes [1]. As depicted in Figure 1, the fundamental structure of an oscillator is a positive feedback network. Numerous engineering systems incorporate a positive feedback cycle. This system would only oscillate under Barkhausen conditions. Equation 1 provides the closed-loop gain [2].

$$\frac{Vo}{Vi} = \frac{A}{1-A\cdot\beta} \quad (1)$$

where A is forward gain and β is the feedback factor.

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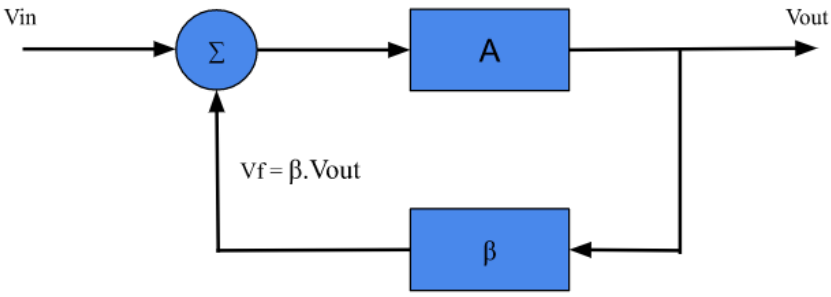

Figure 1. Positive Feedback Network

The simplest feedback oscillator is an Inductor- Capacitor (LC) tank oscillator system. It consists of passive components such as resistors, capacitors, and inductors. Equation 2 gives the frequency (f) of this oscillator with a capacitor (C), inductor (L) [3].

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

1-1- Voltage - Controlled Oscillator

A linear relationship exists between the frequency of a voltage-controlled oscillator and the voltage applied to it. There are two distinct kinds of VCO's: the first is one using a tank circuit, and the second is a ring oscillator. The tank circuit and certain additions make VCO. No matter the kind of oscillator, a VCO functions following Equation 3, which gives the relationship between a control voltage and the resultant frequency. 'ω_o' gives the zero voltage (V_c=0) frequency, and 'k_{vco}' gives the sensitivity or gain of the VCO [4].

The voltage-controlled oscillator operates with a linear relationship between the applied voltage and the frequency of the oscillator, indicating that changing the voltage will cause a corresponding change in the frequency. There are two distinct kinds of VCO's: the first is one using a tank circuit, and the second is a ring oscillator. The operation of a tank oscillator some modifications are required to enable the operation as a VCO. A VCO operates according to Equation 3, which describes the relationship between a control voltage and the generated frequency, or 'ω_{osc}' regardless of the kind of oscillator. 'ω_o' indicates the zero voltage (V_c=0) frequency, while 'k_{vco}' indicates the sensitivity or gain of the VCO [4].

$$w_{osc} = w_o + k_{vco}.V_c \quad (3)$$

Figure 2 gives a diagrammatic representation of the functioning of a VCO. 'ω_{max}' and 'ω_{min}' are the maximum and minimum frequencies respectively, 'V_{min}' and 'V_{max}' are the minimum and maximum voltages, respectively.

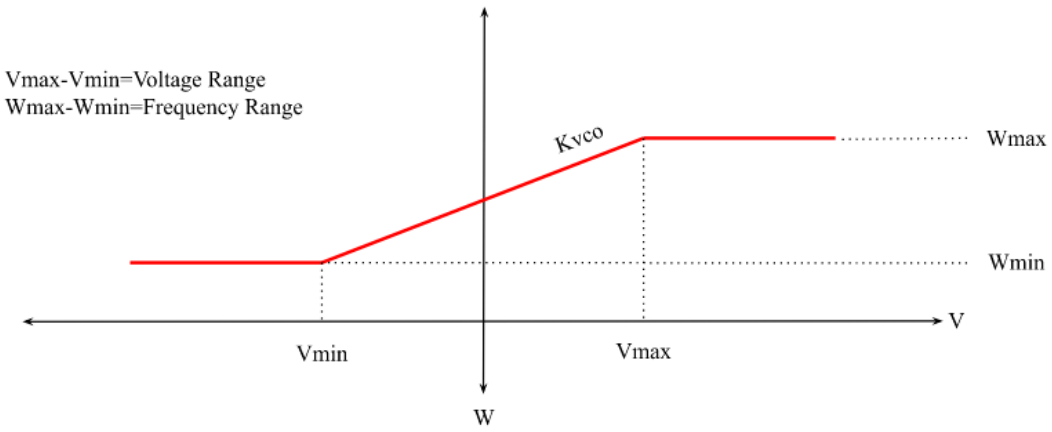

Figure 2. Functioning of a VCO

By utilizing a differential or single-ended inverter, a ring oscillator can be converted into a VCO. Ring oscillators are the most energy-efficient and space-efficient of the two options when compared to tank oscillators. Building ring oscillators using VLSI technology is simple. In conjunction with other electrical components, one can produce ring oscillators. However, ring oscillators and tank oscillators each have drawbacks. Engineers choose ring oscillators with a few modifications to VLSI-based technology [5].

1-2- Ring Oscillator

Combining an odd number of inverting amplifiers creates a ring oscillator. The output from these inverters connects back to the first inverter, creating a positive feedback loop. Amplifiers are always used in conjunction with a self-regulating device because this positive feedback loop is unstable. Figure 3 shows a simplified form of a three-stage ring oscillator. Amplifiers (A), capacitors (C), and resistors (R) make up the various stages. Blowing up an individual amplifier displays the CMOS component as an example. In the common source configuration, the CMOS frequently combines a PMOS and an NMOS. The capacitors provide a delay for the amplifiers, preserving the input within the amplifier for a brief period of time. As a result, the system is able to deliver the necessary delay for the input signal's precise transmission [6]. The capacitors' charging and discharging provide the delay for the inverters. Equation 4, where 'n' is the number of stages, can therefore be used to find the combined delay as follows:

$$f = \frac{1}{n \cdot t_{delay}} \tag{4}$$

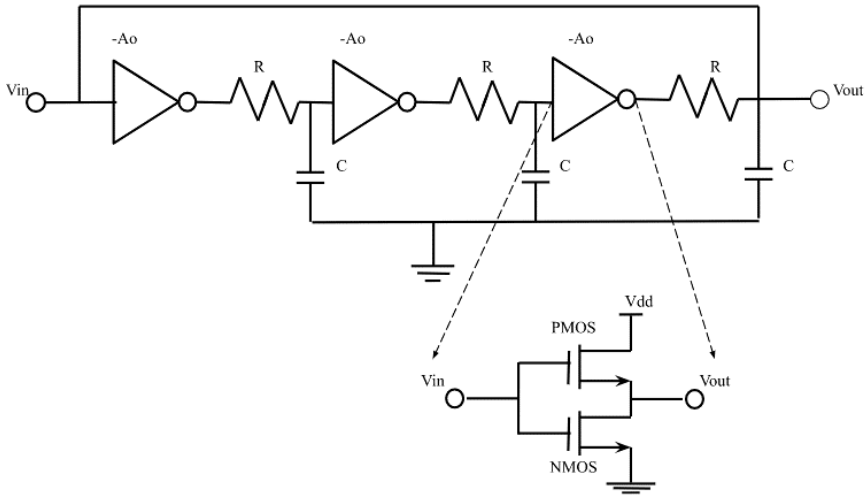

Figure 3. 3 Stage CMOS Ring Oscillator

2- Literature Review

The most important oscillator property for electronics applications is phase noise, often known as jitter [7–10]. These articles offer techniques for physical-based analysis of differential, ring, or CMOS inverter-based oscillators. Additionally, they use time-domain analysis to measure white noise. Jitter noise was connected to the white noise of the circuit, while flicker noise was associated with random VCO modulations. They found white noise during the delay stage and flicker noise during the tuning stage. Routh et al. [11] presented a VCO concept that uses a current mirror to increase drain current. They focused on low-power noise and swing amplitude. The design achieved a power consumption of 6.71 mW and a phase noise of -112 dB/Hz at 180 nm. Designing and analyzing CMOS ring oscillators, such as the standard ring VCO, starved VCO, negative-skewed VCO, etc., was done by Kavyashree et al. [12]. Kavyashree et al. [12] contrasted the results and applicability of each design.

Shekar & Qureshi [13] constructed and investigated a five-stage CMOS inverter VCO. A chain of resistors with a wide NMOS provided linear frequency variation with voltage. They commended the reduced jitter, wide tuning range, and small size of their invention. Additionally evaluated were the power supply, temperature, and corner or process variation. The proposed design had phase noise of -101.9 dB/Hz at 1 MHz offset. A hybrid switching inverter and CMOS ring oscillator were proposed by Kompella and Abdul Rajak [14]. With a small amount of phase and output noise, this design provides a large tuning range. At 1 MHz offset, the output frequency was 2.52 GHz, the settling time was 8.69 ps, and the phase noise was -111 dB/Hz.

Caram et al. [15] described a VCO with an inductive load. In comparison to ring oscillators based on inverters, this improves phase noise and power delivery. Applications determine the development of new oscillator topologies. An innovative VCO made with a 3.5 GHz thin-film bulk acoustic resonator (FBAR) was presented by Hara et al. [16]. Among the advantages of the topology are accuracy, stability, and independence from sequential synchronization. They cite applications including multi-robot coordination, distributed systems, control, and real-time sensor network analysis. Ek et al. [17] built a 28nm FD-SOI CMOS oscillator operating at 26 and 28 GHz. They displayed an integral resolution frequency divider (N-PLL) based on a phased lock loop. Elgaard & Sundstrom [18] suggested a 491.52 MHz FD-SOI

crystal oscillator. The cons of crystal oscillators include higher power consumption, bigger tolerances, and lower Q values. They also employed an amplitude feedback loop to function in linear mode. Abouyoussef et al. [19] suggested using a 5G low-phase noise oscillator. Their design made use of a 14.4 GHz active component and a high-Q quad-spiral microstrip resonator.

Melamed & Cohen [20] discovered the difficulties of 5G wireless communication, particularly free-space route loss. Phased a-ray topologies can overcome these difficulties. They demonstrated a tiny integer N-PLL phase shift technique with a 65-nm, 30-GHz size. Lee et al. [21] described their system's drawbacks, such as a beginning delay and the lack of core transistor bias control. They also offered solutions to these issues, such as an auto-adaptive bias approach, as well as applications of their idea, like a car radar system. A VCO for FMCW radar with a frequency range of 23 to 27.3 GHz was presented by Kumar et al. [22]. It is based on a modified Colpitts differential VCO. Maiellaro et al. [23] developed a frequency splitter. With this information, they built a 40 GHz car VCO. A successful 5G design requires dual-conversion, single-quadrature transceivers. A local oscillator buffer with a balun transformer was presented by Kim et al. [24] to improve the Common Mode Rejection Ratio (CMRR). They added an IF amplifier to a 28-GHz CMOS up-conversion mixer. Kim et al. [25] suggested a 28 GHz direct conversion transceiver. Dan et al. [26] presented THz spectrum applications, such as chip-to-chip communication and long-range modulation for fiber-extended networks. They developed an E-band IF-capable 300-GHz super heterodyne THz connection. Push-push transformer-based oscillators (TBO) were the subject of research by Utomo et al. [27], who discovered power leakage. They discovered methods to reduce power loss, improve DC-RF effectiveness, and increase output power.

According to the literature review, the main difficulties encountered in RF design are power supply, CMOS properties, and phase disturbances. Numerous studies have suggested several design methodologies and architectures that offer answers to these design issues. These studies also described the various applications for the proposed designs, including but not limited to 5G, the Internet of Things, and long-range radio communication. Additionally, a number of studies have emphasized the new 6G telecommunications standard. The RF designs for the aforementioned applications must be dependable and resilient, and voltage-controlled oscillator design is crucial to this. All radio communication relies on the operation of a VCO; thus, it requires the right specs and design. Ciarpi et al. [28] showcased that RO-VCO exhibits a frequency tuning range spanning from 4.72 GHz to 6.12 GHz. The structure consists of three closed-loop differential stages that are asymmetrical. Using the given data, the phase noise and figure of merit were calculated to be -103.2 and -186.2%, respectively, at a frequency offset of 1 MHz from the 5.5 GHz carrier. Furthermore, a thorough analysis and demonstration of the practical assessment of the constructed device's thermal and electrical properties are provided. The research work presented by Hemel et al. [29] on the design of a voltage-controlled oscillator (VCO) using a single-ended ring oscillator (RO) configuration. The purpose of the RO-VCO was to achieve extensive compatibility with an Internet of Things (IoT) wireless health monitoring system. The concept was constructed using 50 nm CMOS technology. To initiate the voltage-controlled oscillator within the frequency range of 1.67 to 3.13 GHz, adjust the control voltage within the range of 0.9 V to 1.5 V. A supply voltage of one volt generated an oscillation of 2.4 GHz.

Rahim et al. [30] designed a three-stage oscillator that oscillates from 19.75 GHz to 178.71 GHz, depending on the control voltage. HSPICE simulations with 16 nm MOS-GNRFET technology and 0.8 V supply voltage yielded the result. The investigated voltage-controlled resonator (VCRO) uses only 1.33 microwatts (μW) of power across all frequency modifications. The power-delay product (PDP) was vital to this study. The suggested oscillator reached 1.24 aJ for this metric. This finding was based on frequency tuning range data. A cascaded wideband local oscillation generator designed by Jo et al. [31] with extremely low interference is presented here. The generator works at 5G FR1. The phase-rotating divider (PRD) function in the second-stage ring-oscillator-based frequency multiplier (RO-FM) reduced the first-stage phase-locked loop (PLL) frequency-tuning range (FTR) by 21%. PRD was used to generate fractional multiplication factors (Ms). A single low-phase-noise voltage-controlled oscillator (VCO) can solve this problem. A cascaded local oscillation (LO) generator designed by Sivasakthi & Radhika [32] generates ultra-low-jitter wideband signals for 5G FR1. The ring-oscillator-based second-stage frequency multiplier generated fractional multiplication factors using a phase-rotating divider. This cut the first-stage phase-locked loop's frequency-tuning range by 21%. A single VCO can cover this range for low-phase noise LC.

3- Various Voltage-Controlled Oscillator Structures and their Implementation

3-1- Conventional Ring CMOS VCO

The basic design of a ring VCO is this type of ring oscillator, as illustrated in Figure 2, which has a straightforward structure. An additional component in the circuit controls the bias voltage, which is being mimicked here. In order to evaluate the best performance, this design was constructed on a typical 50nm node without taking the oscillation frequency or waveform into account. The actual design that was used is displayed in Figure 4. Figure 5 shows the oscillation frequency of 7.15 GHz in the output waveform.

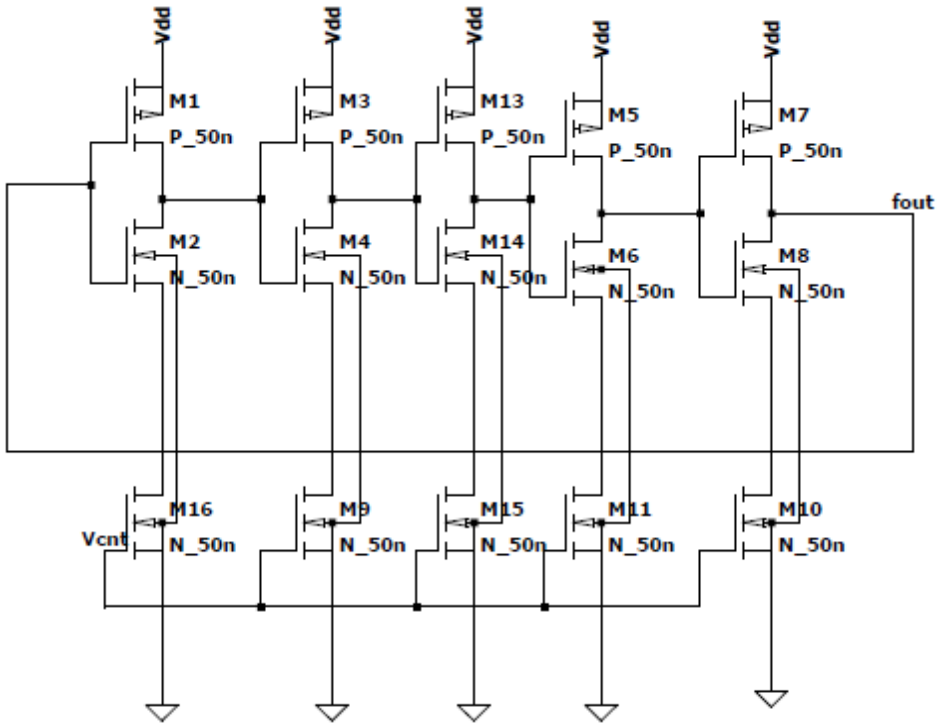

Figure 4. CMOS Ring Oscillator Simulated

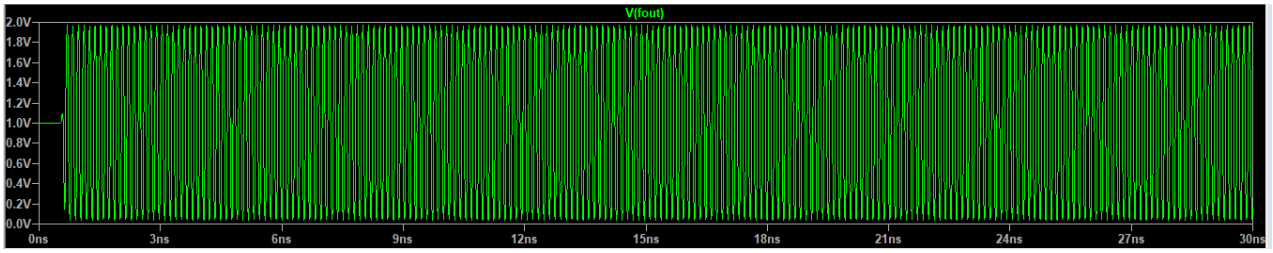

Figure 5. Output Waveform of CMOS Ring Oscillator

The delay of all the different stages combined gives the frequency of operation for this circuit. The common source arrangement of these devices uses CMOS; hence, the delay durations between the low and high states will vary. Equations 5 and 6 show the temporal delays from high to low (τ_{dhl}) and low to high (τ_{dlh}), respectively. In these equations, k_n and k_p represent the internal resistance, V_{dd} represents the bias voltage, and V_{tn} and V_{pn} represent the NMOS and PMOS terminal voltages [7].

$$\tau_{dhl} = \frac{c}{k_n(V_{dd}-V_{tn})}\left(\frac{2V_{tn}}{V_{dd}-V_{tn}} + \ln\frac{3V_{dd}-4V_{tn}}{V_{dd}}\right) \quad (5)$$

$$\tau_{dlh} = \frac{c}{k_p(V_{dd}+V_{tp})}\left(\frac{2V_{tp}}{V_{dd}+V_{tp}} + \ln\frac{3V_{dd}-4V_{tp}}{V_{dd}}\right) \quad (6)$$

The total delay τ_d is then computed through the average of both delays, given through Equation 7,

$$\tau_d = \frac{\tau_{dhl}+\tau_{dlh}}{2} \quad (7)$$

The frequency of operation is found using Equation 3 because the basic time delay theory is the same for any kind of oscillator system. Some phase noise is observed and can be approximated at 35.33% due to the difference in phase between the harmonic components.

3-2- Negative Skewed CMOS Ring VCO

The large delay time of typical ring VCOs is a significant drawback. A negative-skewed VCO can get rid of this. This entails simply the PMOS portion of the CMOS receiving a delay. This enables the system as a whole to produce the intended results more quickly. But in order for this delay to work, it also needs a greater oscillation frequency and a little bit more power input. In order to evaluate the best performance, this design was constructed on a typical 50nm node without taking the oscillation frequency or waveform into account. The schematic diagram of the two-stage delay,

negative skewed delay, and standard ring oscillator circuit for the negative skewed CMOS ring VCO is shown in Figure 6. Figure 7 shows the output waveform, indicating an oscillation frequency of 3.35 GHz.

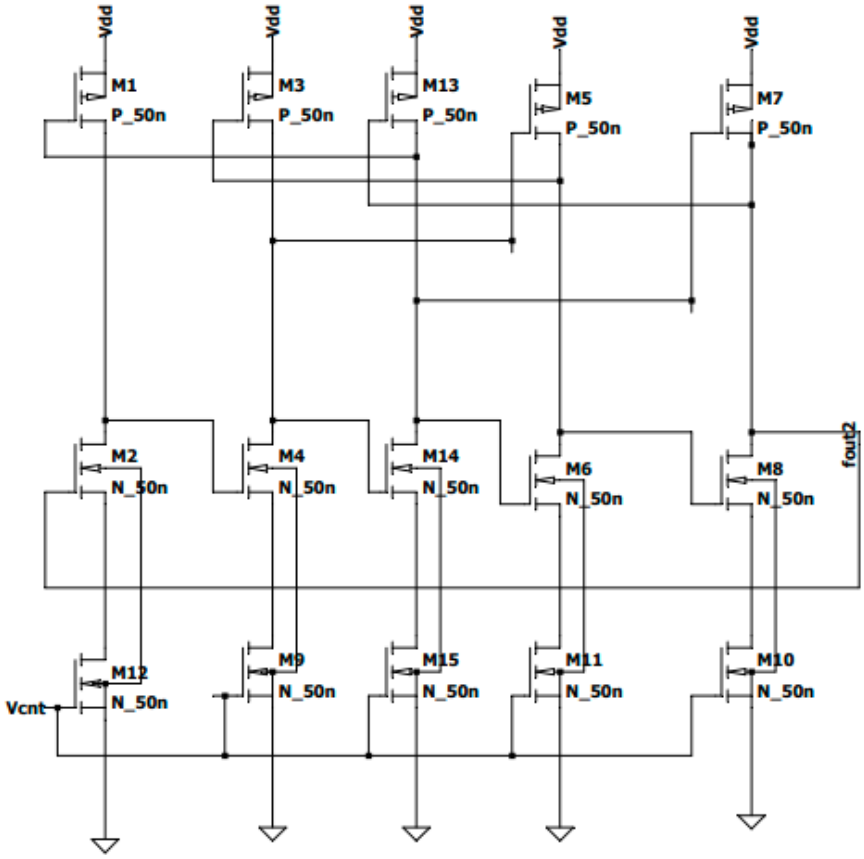

Figure 6. Negative Skewed CMOS Ring Oscillator Simulated

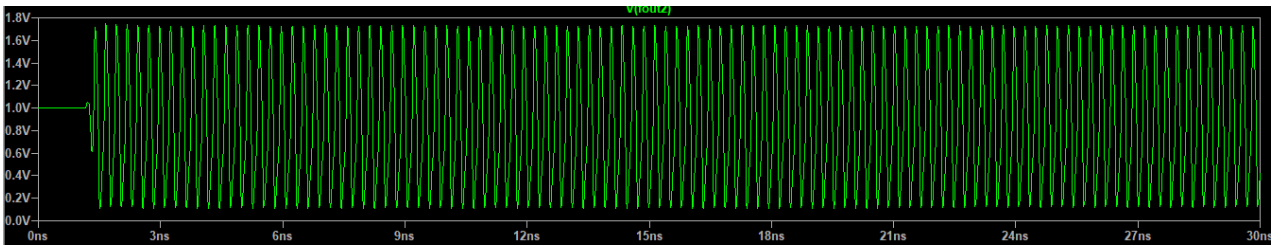

Figure 7. Output Waveform of Negative Skewed CMOS Ring Oscillator

This configuration's delay and frequency calculations are identical to those for the standard arrangement, with the additional delay added in Equation 3 [7]. The results unmistakably demonstrate that the design can exhibit better reactions and reduced delay while retaining the issue that the typical ring VCO faces due to excessive phase noises. A 36.62% overall harmonic distortion is observed.

3-3- Current Starved CMOS Ring VCO

The absence of current regulation and moderation is the main flaw in the prior two CMOS systems. However, by increasing the number of CMOS and altering their functionality to match that of current sinks and drains attached to standard inverters. A current source that also serves as a current limiter will be present in each inverter. Additionally, the inverters are equipped with comparable drains to allow for the extraction of any excess current. As a result, current is scarce for all inverters. The supply voltage "V_{dd}" determines the amount of current that is drawn. The design's lower current requirement reduces phase noise and power consumption. Moreover, traversing more branches of the circuit with the current enhances the overall production of the output waveform. However, there is a greater need for space because numerous CMOS transistors are necessary. In order to evaluate the best performance, this design was constructed on a typical 50nm node without taking the oscillation frequency or waveform into account. Figure 8 displays the implemented design. Figure 9 displays the output waveform, indicating a frequency of oscillation of 2.3 GHz.

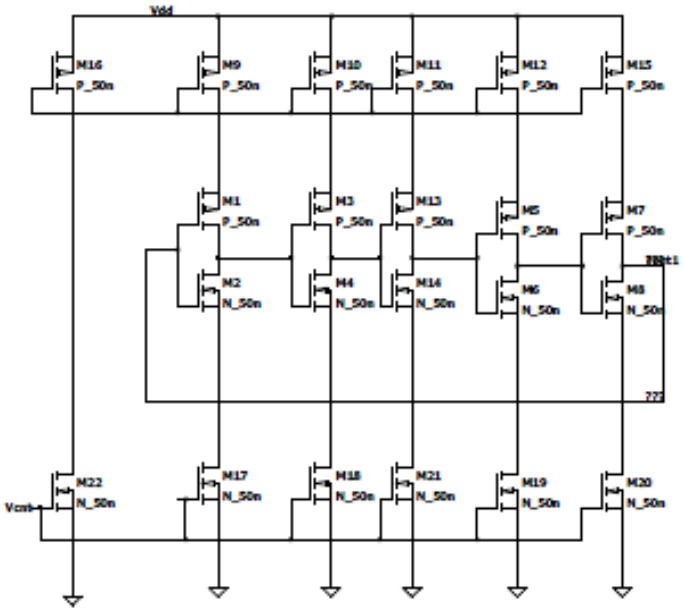

Figure 8. Current Starved CMOS Ring VCO Simulated

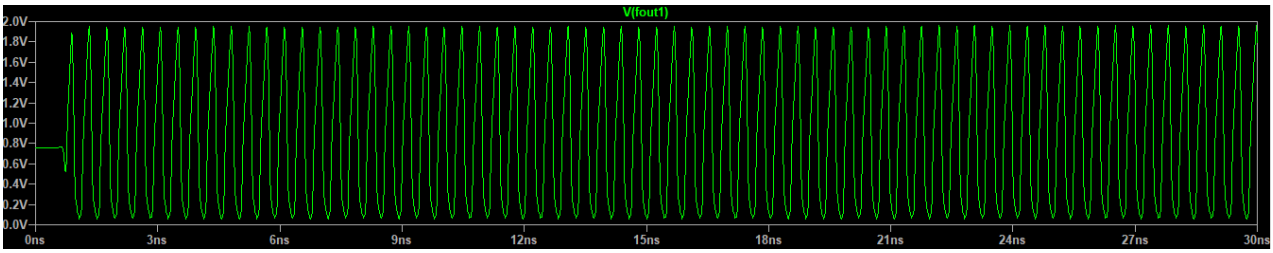

Figure 9. Output Waveform of Current Starved CMOS VCO

The inclusion of current sinks and drains adds an additional capacitive component to the delay calculations. The oxide layers, in which the capacitances (C'_{ox}) must be replaced based on research from BSIM4 models, will affect these capacitive components. Equation 8 gives the total capacitance, where 'C_{in}' and 'C_{out}' are the input and output capacitance of the inverters, respectively; width (W_p) and length (L_p) are the dimensions of the PMOS, and width (W_n) and length (L_n) are the dimensions of the PMOS NMOS components, respectively [7].

$$C_{tot} = C_{out} + C_{in} \Rightarrow C_{tot} = C'_{ox}\left(W_pL_p + W_nL_n\right) + \frac{3}{2}C'_{ox}\left(W_pL_p + W_nL_n\right)$$
$$\Rightarrow C_{tot} = \frac{5}{2}C'_{ox}\left(W_pL_p + W_nL_n\right) \quad (8)$$

The delay can then be found through Equation 9, where 'N' represents the number of stages in the design, 'I_d' represents the drain current due to supply voltage 'V_{dd}' [33], and the frequency of oscillation f_{osc} is given by;

$$f_{osc} = \frac{I_d}{N.C_{tot}.V_{dd}} \quad (9)$$

The findings indicate that the measured phase noise and subsequent harmonic distortion are 25.41% lower compared to a traditional CMOS ring VCO. However, the oscillation frequencies are considerably lower than those of the earlier designs.

3-4- Comparison and Analysis of Results from Implementation of Various VCOs

The simulations demonstrated the wide range of CMOS amplifier-based ring VCO configurations that are possible. We examined the advantages and disadvantages of these configurations, as well as the design process, simulation findings, and implementation. The following characteristics were noticed following simulations of the three distinctive designs, conventional ring, negative skewed, and current starved.

The decision-making process for design characteristics including transistor technology, frequency, and power ensures that all three configurations may be properly analyzed. The utilized transistors have dimensions of 50 nm, L_n=50 nm, W_n=500 nm, L_P=50 nm, and W_P=1 m. All variants used a 2 V power supply, as shown by the value of 'V_{dd}'. All designs had a control voltage of 1.15 V, with the exception of the negative skewed ring VCO, which had a control voltage of 1.36 V. For all designs, there were meant to be five stages.

High-phase noise, a lack of current regulation, and a lengthy response time are considered the drawbacks of the traditional CMOS ring design. The modifications to the negatively skewed CMOS design, which also lessen frequency variation and phase noise, can address the shorter response time. The power requirement is still larger, and frequency jittering noise is still present. A traditional design's conversion to a current-starved CMOS results in improvements that reduce phase noise, which improves the waveform. Additionally, the current starved design has shown a decrease in power requirements. The inclusion and placement of additional transistors explain both outcomes. Both outcomes are explained by the inclusion and placement of additional transistors. Furthermore, the frequencies are lowered by the number of transistors. When compared to the conventional design, the adjustments made to achieve the negative skewed ring VCO allow for a significantly faster response time. Furthermore, the findings demonstrate a reduction in frequency variation and improved handling of phase noise caused by phase differences between stages. However, this design does not manage power as effectively as previous designs since it needs a slightly higher control voltage and current.

4- Problem Statement

We conducted a comprehensive analysis to examine the operational capabilities and characteristics of numerous ring oscillators based on complementary metal-oxide-semiconductor (CMOS) technology. This inquiry involved a combination of computer simulations and an extensive review of pertinent literature. The merits and disadvantages of each article were emphasized, and the study also presented detailed information regarding the design methodology employed in the construction of each architectural structure. Furthermore, the literature review has indicated a scarcity of CMOS ring voltage-controlled oscillators (VCOs) that are appropriate for implementation in 5G mobile communication applications. Consequently, the suggested design was subjected to modeling and simulation, with a primary focus on achieving reduced phase noise, minimal power consumption, and the ability to customize frequencies.

5- Design of Proposed Current Starved, Negative Skewed Ring Voltage-Controlled Oscillator

5-1- Design Procedure and Considerations for Proposed Architecture

When creating a CMOS oscillator, there are three main factors to consider. They are the characteristics of the CMOSs being utilized, the frequency of oscillation, and the quantity of stages being employed. Numerous of these factors are also interrelated and changeable, as shown in Figure 10. Therefore, one must choose the various parameters in accordance with the specifications and performance outcomes. For CMOS in the common source design, an increase in frequency causes an increase in capacitance. Phase noise for the CMOS will increase with a drop-in supply voltage (V_{dd}). As a result, the primary design parameter for CMOS devices must be their sensitivity to supply fluctuations. These are possible formulations:

- By selecting higher W/L ratios and the longest practicable channel length (L), we can decrease noise [34];
- Other elements affecting the choice of operating frequency prevent the determination of frequency based on the CMOS's capacitance fluctuations. To account for any additional capacitance caused by the frequency choices, it is necessary to appropriately select the individual capacitors.

There are numerous influencing elements when choosing a frequency. These factors, as previously noted, are dependent on the operation of an oscillator, as shown in Equations 2 to 5, and they are also based on the saturation of the employed CMOSs. It is possible to state the frequency selection as follows:

- The operational frequency will rise as the voltage increases. Following Equation 5, adjusting the capacitors will vary the frequency through a change in the capacitance delay 't_{delay}'. However, this is constrained by the saturation level of the CMOSs being utilized [7].
- The main constraint on the practical frequency choice is the use of the oscillator. It is necessary to select frequencies appropriately because some applications call for particular ones.

As already said, the main restriction on frequency selection is the application. By selecting the proper capacitors and supply voltages, the other frequency-influencing factors can be removed.

For CMOS ring oscillators, the number of stages is a very unstable design parameter. Changes in the number of stages, whether increased or decreased, significantly affect power, frequency, and noise. The modifications are as follows:

- The frequency will decrease as the number of phases increases. This is because the increased number of stages provides a longer delay.
- The need for power will increase as the number of phases rises.
- An increase in the number of stages will result in reduced dissipated power [34]. This is because more CMOSs are being utilized in the circuit.

Figure 10. Flowchart of Design

Table 1 provides the specifications for the suggested design based on various iterations and comparisons with comparable designs.

Table 1. Specifications of Design

Parameter	Value
Supply Power (V_{dd})	2 V
Control Voltage	1.15 V
CMOS Transistor	50 nm
Number of Stages	5

5-2- Modeling of Proposed Architecture

The suggested architecture aimed to utilize the knowledge gained from the distinctive designs. The proposed design aims to develop a system that allows for the use of advantages while removing downsides. Application of the design within 5G devices was a key necessity. Therefore, the design's size, frequency, and power requirements are essential. Figure 11 depicts the proposed architectural schematic, which draws inspiration from both existing starving and negatively skewed constructions.

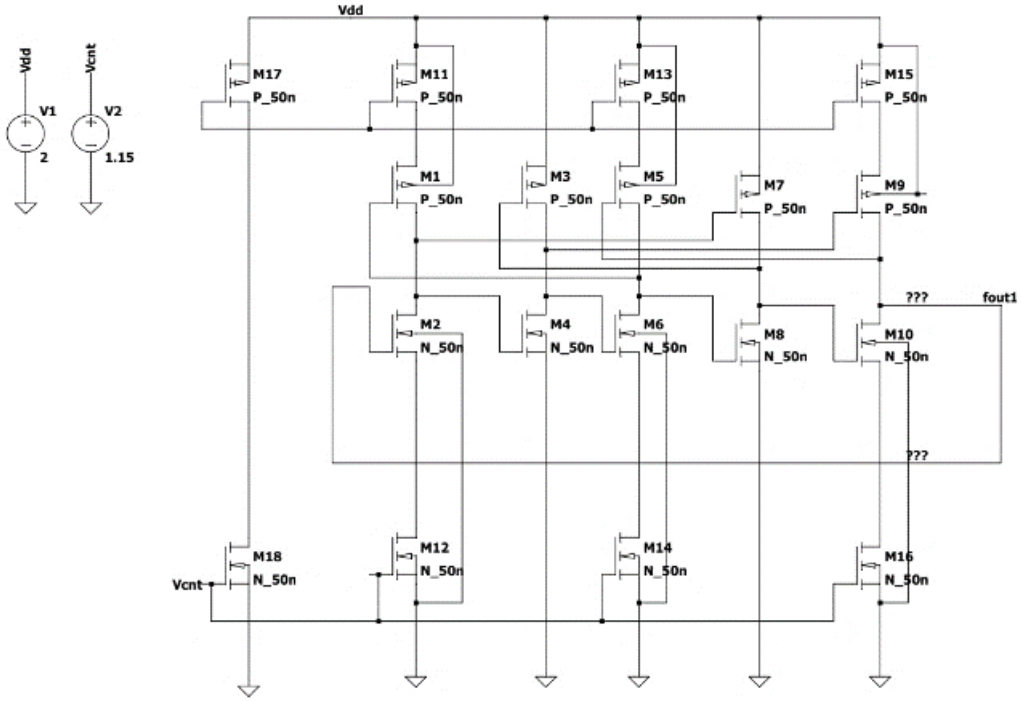

Figure 11. Schematic of Proposed Design

Each CMOS works in the manner described below: Negative skewed delay oscillators are found in CMOS M1 through M10; current-limited oscillators are found in CMOS M11 through M16; and biasing or control circuits are found in CMOS M17 and M18. Five-stage inverters M11 through M19 are available. The current limiters or outlets M11 to M19 limit the current of three successive stages—the first, third, and fifth stages. This current constraint enables the topology to achieve the best possible power usage. By setting the operational voltage, M20 and M21 act as current sources as well as the control or biasing circuit for the topology.

The proposed design's delay computation requires computing the delay for each of the design's architectures independently. Equations 6 to 8 give the negative skewed component of the circuit's delay. Equations 9 and 10 provide

the delay of the circuit's current-starved portion Equation 11 determines the total delay, where 'τ_d' represents the overall delay, 'τ_{cs}' represents the current starving delay, 'τ_{ns}' represents the negative skewed delay, and 'N_1' and 'N_2' represent the number of stages for the current famished form and the negative skewed form, respectively.

$$\tau_d = N_1\tau_{cs} + N_2\tau_{ns} \tag{11}$$

Figure 12 depicts the proposed architecture implemented using LTspice to acquire the results of waveform, rapid Fourier transform, harmonic distortion, and harmonic frequencies. LTspice reports revealed additional frequency divisions and components. Through LTspice reports, more frequency divisions and components were discovered. With L_n = 50 nm, W_n = 500 nm, L_P = 50 nm, and W_P = 1 m, the simulation was performed on a 50 nm technology. The power requirement was chosen and modified in response to the outcomes. The previously discussed architectures and the suggested architecture were contrasted in terms of harmonic distortion, power consumption, and frequency.

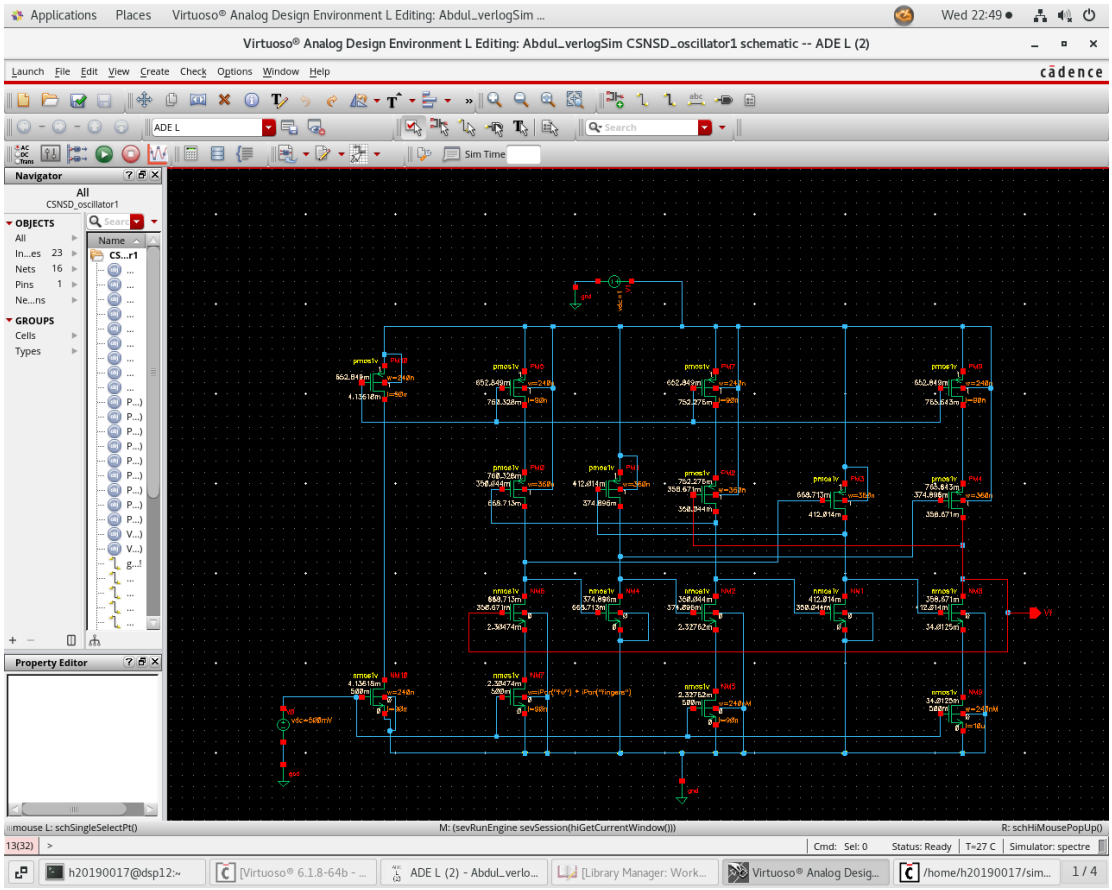

Figure 12. Proposed Architecture

Figure 13 shows the output waveform obtained. The maximum voltage can be observed as 1 V. The frequency is higher than all other architectures studied through implementation.

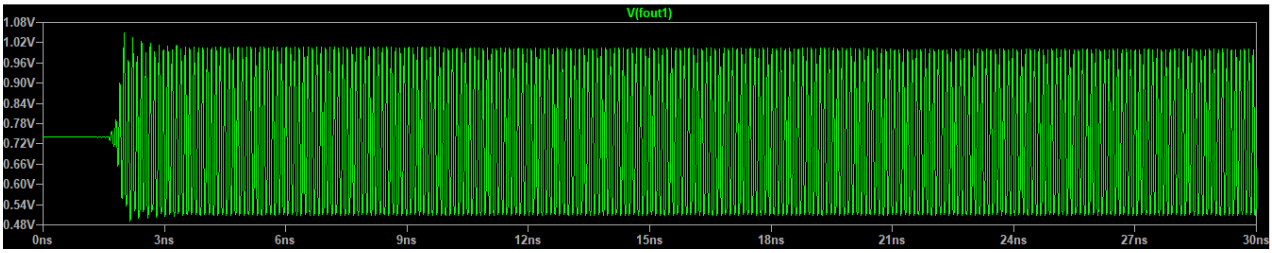

Figure 13. Output Waveform of Proposed Architecture

6- Results and Discussion of Proposed Architecture

The waveform obtained as output is shown in Figure 13. The maximum voltage that can be served is one volt. This architecture has a higher frequency compared to other investigated architectures.

Figure 14 illustrates the range of frequencies that the suggested design can produce through its FFT output. It turns out that 9.35 GHz is the most important frequency. Even more encouraging for 5G-related uses is the existence of numerous frequencies over a broad range.

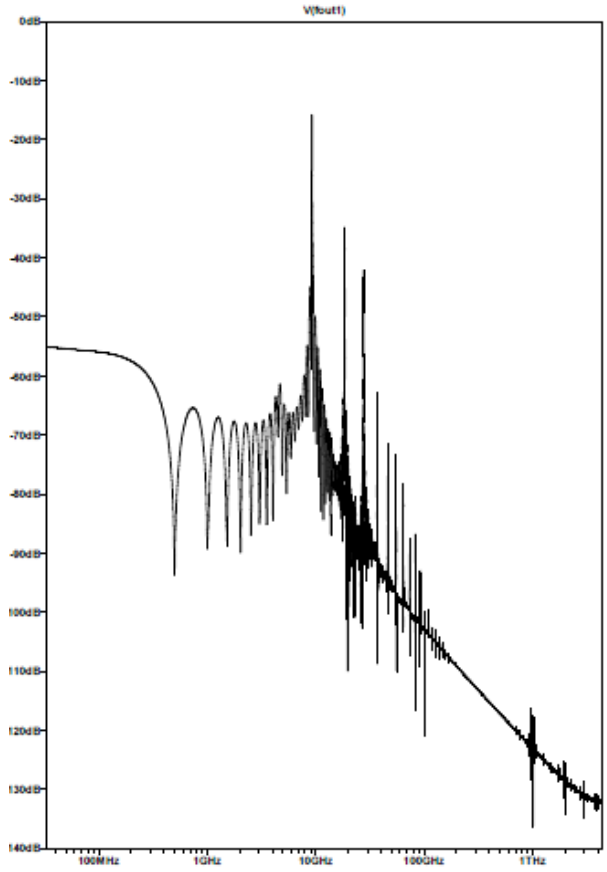

Figure 14. FFT result of proposed architecture

Figure 15 illustrates the LTspice simulation outcome, presenting the distinct harmonic frequencies up to the fifth harmonic, the total harmonic distortion, the Fourier component, the normalized component, and the phase degree of each unique harmonic. The measurement of overall harmonic distortion yielded a value of 13.82%. The frequency of oscillation in the current architectures is higher compared to those in previous designs, as illustrated in Table 2.

Fourier components of V(fout1)
DC component:0.724384

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	9.356e+09	2.738e-01	1.000e+00	-86.59°	0.00°
2	1.871e+10	3.408e-02	1.245e-01	72.11°	158.70°
3	2.807e+10	1.603e-02	5.857e-02	117.19°	203.78°
4	3.742e+10	3.519e-03	1.285e-02	104.42°	191.00°
5	4.678e+10	1.227e-03	4.482e-03	-126.82°	-40.23°

Total Harmonic Distortion: 13.825059%(13.881148%)

Figure 15. LTspice Log Analysis Report of Proposed Architecture

Table 2. Specifications of Proposed Architecture

Parameter/ Architecture	Supply Voltage (Vd)	Control Voltage (Vc)	1st Harmonic (GHz)	2nd Harmonic (GHz)	3rd Harmonic (GHz)	4th Harmonic (GHz)	Harmonic Distortion (%)
Conventional	2	1.15	7.15	14.3	21.45	28.6	35.33
Current Starved	2	1.15	2.3	4.6	6.9	9.2	25.41
Negative Skewed	2	1.65	3.35	6.7	10.05	13.4	36.62
Proposed Architecture	2	1.15	9.35	18.71	28.07	37.42	13.82

The performance comparison of the proposed architecture with other architectures that were evaluated for investigation is presented in Table 2.

As was said earlier, the suggested architecture is capable of being utilized for 5G application deployments. The steps outlined below are an example of a design process for an application operating at a frequency of 27.7 GHz, which was picked at random. Using Equation 12, and assuming that the frequency of the application is already known, one can get the individual delays for the negatively skewed sections and the current-starved parts as follows:

$$\frac{1}{27.7\times10^{9}} = N_1\tau_{cs} + N_2\tau_{ns} \Rightarrow N_1\tau_{cs} + N_2\tau_{ns} = 0.0361\ ns \tag{12}$$

The particular application must be taken into consideration before deciding on the number of stages that will be used for each component, which is denoted by N_1 and N_2. If N_1=3, N_2=2, and the total number of stages is N=5, then Equation 13 will indicate the relation between the individual delays and the total delay for the stage.

$$\begin{aligned}\tau_{cs} &= \frac{N_1}{N}\tau_d \Rightarrow \tau_{cs} = \frac{3}{5}(36.1\times10^{-12}) \Rightarrow \tau_{cs} = 0.0223\ ns\\ \tau_{ns} &= \frac{N_2}{N}\tau_d \Rightarrow \tau_{ns} = \frac{2}{5}(36.1\times10^{-12}) \Rightarrow \tau_{ns} = 0.0145\ ns\end{aligned} \tag{13}$$

After computing the individual delays, the operational parameters of the currently starved and negatively skewed parts are computed. From Equation 14, where Id is the saturation current, the total capacitance can be found as follows:

$$C_{tot} = \frac{\tau_{cs}I_d}{N_1V_{dd}} \Rightarrow C = 0.0223ns \times \frac{360\mu A}{2V} \Rightarrow C = 0.3999fF \tag{14}$$

From Equation 15, the individual capacitance can be found as follows,

$$C_{tot} = \frac{5}{2}C'_{ox}\left(W_pL_p + W_nL_n\right) \Rightarrow C'_{ox} = 0.0159fF \tag{15}$$

From Equation 8, the total delay of negative skewed portion allows the computation of the high to low and low to high delays, where for simplicity's sake they are taken as the same, as seen in Equation 16,

$$\tau_{ns} = \frac{\tau_{dlh}+\tau_{dhl}}{2N_2} \Rightarrow \tau_{dlh} = \tau_{dlh} = 0.0072ns \tag{16}$$

From Equations 7 and 8, the operating capacitance of the negative skewed portion can be computed in Equation 17, with transistor parameters V_d=2V and V_{tp}=V_{tn}=0.3V,

$$\frac{c}{k_p} = \frac{\tau_{dlh}(V_{dd}+V_{tp})}{\left(\frac{2V_{tp}}{V_{dd}+V_{tp}}+\ln\frac{3V_{dd}-4V_{tp}}{V_{dd}}\right)};\frac{c}{k_n} = \frac{\tau_{dhl}(V_{dd}-V_{tn})}{\left(\frac{2V_{tn}}{V_{dd}-V_{tn}}+\ln\frac{3V_{dd}-4V_{tn}}{V_{dd}}\right)} \Rightarrow \frac{c}{k_p} = \frac{c}{k_n} = \frac{0.0123\times10^{-9}}{0.3529\times\ln2.4} = 0.0397\times10^{-9}sV \tag{17}$$

Thus, according to the application, the design can be modelled for specific requirements and adjusted to achieve results.

7- Conclusion

The transceiver for 5G standard mobile communication employs a VCO with a large tuning range and a short settling time. This VCO should also have low-phase noise for improved performance. With 5G technologies and IoT applications, it is possible to build smart homes, smart cities, smart cars, smart grids, and health care services. Due to the use of several architectural styles, the current starving design was able to create the least amount of harmonic distortion, but at the sacrifice of the frequency range and the amount of area it took up. However, a negative skew design improves the frequencies that can be reached, but it comes with the trade-off of requiring a higher control voltage and resulting in increased harmonic distortion. In comparison to alternative architectures, the suggested architecture was successful in producing lower harmonic distortion while still ensuring higher frequencies that are suitable for 5G-based applications that need low-power circuits and high-frequency operation. With this approach, power is used more effectively and can be controlled at lower voltages. For the proposed architecture, it was predicted that the supply voltage would be 2 V and the control voltage would be 1.15 V. 9.35, 18.71, and 28.07 GHz were produced by the architecture with just 13.82% harmonic distortion between the inputs and outputs. Furthermore, the interaction of current-starved and negatively skewed topologies allows for the implementation of the recommended architecture for 5G-based applications by carefully selecting the passive components included in the design.

8- Declarations

8-1-Author Contributions

Conceptualization, A.R., S.K., and A.R.A.R.; methodology, A.R.; software, A.R.; validation, A.R., S.K. and A.R.A.R.; formal analysis, A.R. and A.R.A.R.; investigation, A.R.; resources, A.R.; data curation, A.R.; writing—original draft preparation, A.R., S.K., and A.R.A.R.; writing—review and editing, A.R., S.K., and A.R.A.R.; visualization, A.R..; supervision, A.R.A.R.; project administration, A.R.A.R.; funding acquisition, A.R.A.R. All authors have read and agreed to the published version of the manuscript.

8-2- Data Availability Statement

The data presented in this study are available on request from the corresponding author.

8-3- Funding

The authors received no financial support for the research, authorship, and/or publication of this article.

8-4- Institutional Review Board Statement

Not applicable.

8-5- Informed Consent Statement

Not applicable.

8-6- Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancies have been completely observed by the authors.

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