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BIST-based Testing and Diagnosis of LUTs in SRAM-based FPGAs

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Abstract

FPGA chips have wide applications in nowadays digital systems. Because of fault prone nature of FPGA chips, testing of them is one of the major challenges for designers. Among various test methods, the Built-in Self-Test (BIST) based ones have shown good performance. In this paper, we presented a BIST-based approach to test LUTs as most vulnerable part of FPGA chip. The BIST-based approach is off-line and has been accomplished within two FPGA configurations. Each configurable logic block (CLB) can be tested independently and there is no handshaking among various CLBs' BIST cores. The proposed BIST architecture has been simulated in HSPICE based on 45-nm CMOS technology. Simulation results shown 100% coverage for single stuck at faults along with 19% area overhead due to additional BIST hardware and 25% increase in leakage power.

Keywords:

FPGA;
Internal Testing;
BIST;
Test Pattern Generator;
LUT.

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1- Introduction

FPGA (Field Programmable Gate Array) chips have become an important part in modern digital systems. In-field re-configurability of these chips has shortened the time to market for most applications. On the other hand, shrinking the feature size of transistors in modern CMOS technologies imposes many challenges for detection and diagnosis of defects in FPGA chips. Various test approaches for FPGA chips have been developed in recent decades. Test time and cost are two important factors for these testing scenarios [1, 2].

BIST as a testing method for logic circuits has been widely used [3-6]. In last two decades different BIST architectures have been developed for FPGA testing; each of them has some pros and cons [7-9]. Various methods have been proposed to test CLB. These methods are different in test time and the number of required CLB configurations. A large portion of these methods is based on external testing and some are concerned with Design for Testability (DFT). BIST as an efficient testing method is based on constructing a hardware core in CMOS-chip to make the testing operation internally [10]. The main parts of BIST architecture illustrated in Figure 1.

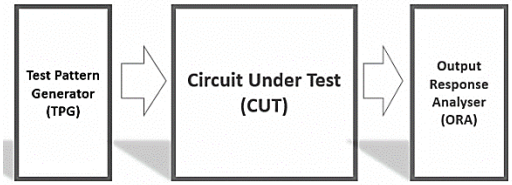

Figure 1. General structure for BIST test.

Test Pattern Generator (TPG) generates required test vectors (exhaustively, randomly…) then these vectors apply to the Circuit Under Test (CUT) and finally using Output Response Analyser (ORA) the CUT output values are compared with expected values and for each test vector Pass/Fail state of CUT will be determined.

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1-1- Related Works

The early studies on BIST-based FPGA testing have been concerned the architecture of hardware resources which can be used to test the FPGA internal circuitry. For example, in [3] shift registers have been used to generate the random pattern and signature as well as response analyser. In [4] linear-feedback-shift-register (LFSR) has been used to develop TPG and ORA. An efficient and fast method has been developed for delay fault testing in [6]. Abramovici and Stroude [11] presented a BIST approach which can detect and diagnosis all LB faults, but their method needs several FPGA re-configurations which makes this method very time consuming. A modification of the above method has been presented in [12] with lower number of reconfigurations. In [13] a method to test the delay faults has been developed which is exhaustive and cost efficient. A testing architecture has been presented in [14] which detect and diagnosis single and multiple fault in LUTs. In this test method the ORA has been placed into the FPGA chip. Smith et al. (2006) has presented a BIST approach to test delay and interconnect faults in FPGA [15]. In [16] the test strategy for detection and diagnosis of LB's faults has been developed which is very fast and has a high coverage rate. An approach with 17 configurations has been presented in [17] which can cover 100% of faults in LUTs. To test the memory block of FPGA a reconfigurable BIST architecture has been developed in [18]. In [19] a power aware test method has been presented in which required test patterns have been generated to reduce the switching activity of circuit during test time. This method leads to 49- 77 % reduction in power dissipation of some benchmark circuits testing. A novel BIST based approach has been developed in [20] in which TPG and ORA have been implemented in software part but the CUT implemented in hardware form. Another FPGA has been used for TPG and ORA and two communication channels connect these two parts to CUT. In [21] an off-line interconnects test methodology has been developed which efficiently covered crosstalk faults in FPGA. In [22] an improved BIST architecture has been presented which uses minimum reconfiguration and can detect LUT and interconnections faults. In [23] a BIST-based implementation of multiplier blocks of FPGA has been presented.

2- Proposed BIST Architecture

FPGA chip generally is a 2-D array of Configurable Logic Blocks (CLB) surrounded by Input-Output (IO) blocks (Figure 2).

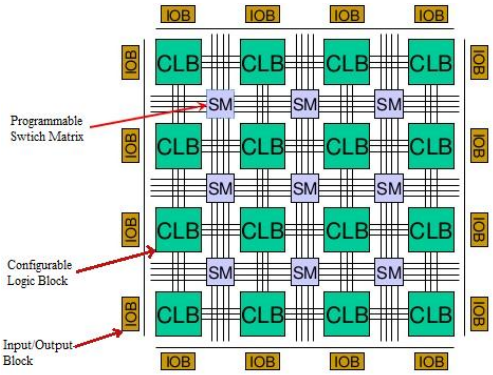

Figure 2. Architecture of SRAM-based FPGA.

Horizontal and vertical channels are used to connect the above resources. Switch Blocks (SB) which have been put on cross-sections of horizontal and vertical channels can be configured to make required routing properly [24]. In this paper a CLB consists of four logic blocks (LB) (Figure 3).

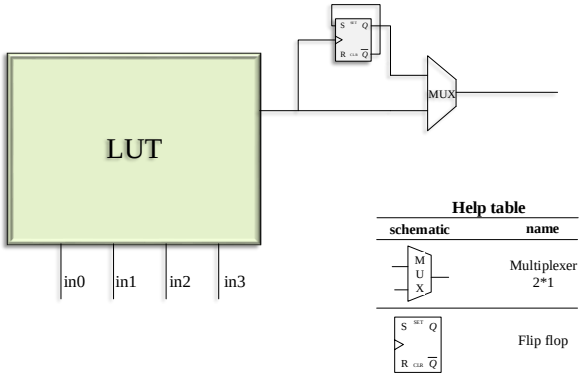

Figure 3. The structure of an LB.

A logic block consists of a 4-input Look-Up Table (LUT), a DFF and a multiplexer. The input channel of LB is directly connected to input lines of LUT. Using the LB's multiplexer, the output of LUT can be registered (using DFF) or can be directly connected to the output of LB. A 4-input LUT can implement any 4-input switching function. The truth table of such functions is stored in 16 SRAM-cells in LUT and the output lines of these SRAM-cells connect to the LUT's output using a $2^4 \times 1$ multiplexer [25]. LUT architecture has been illustrated in Figure 4.

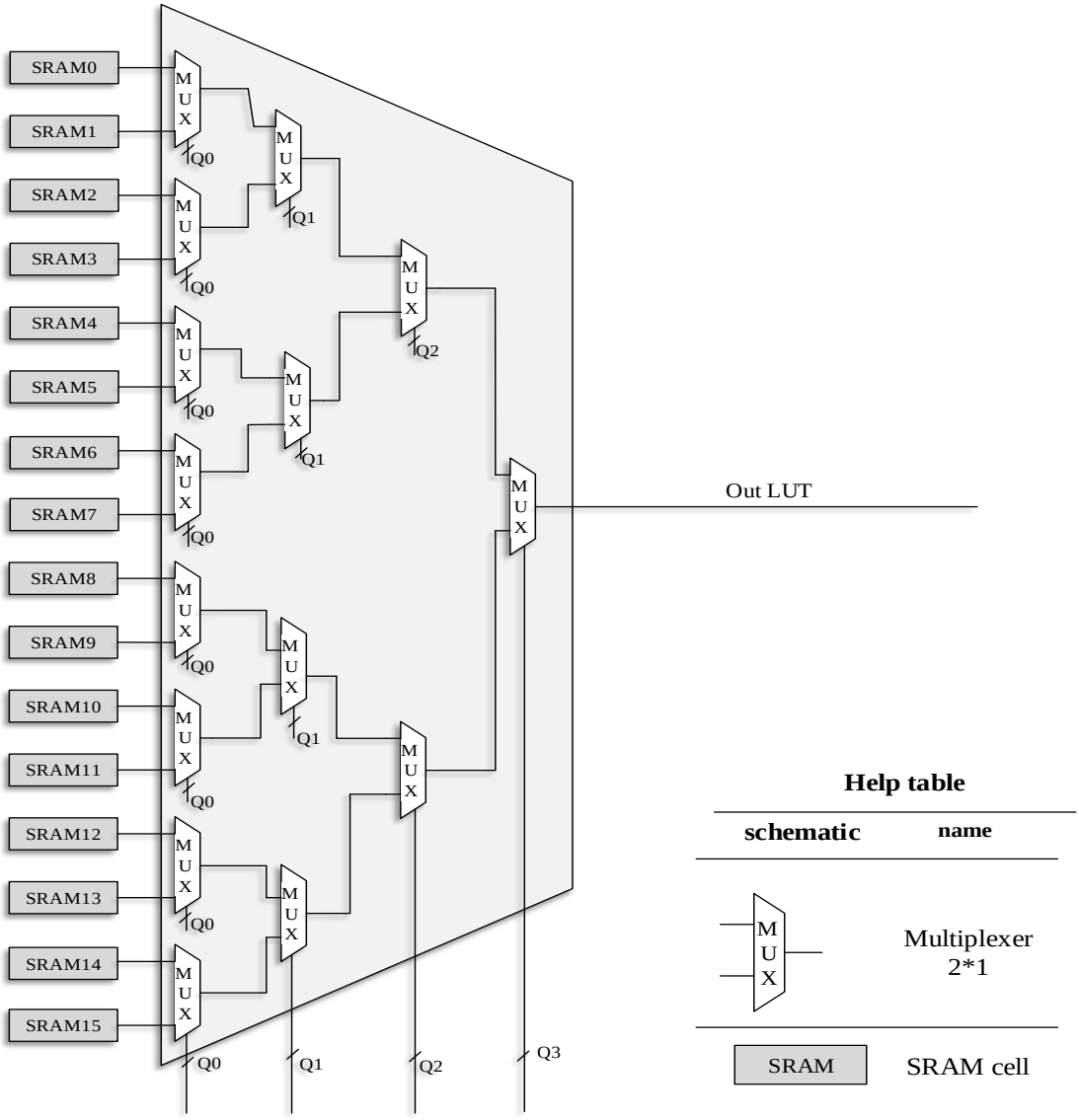

Figure 4. The structure of a LUT.

Initially, in our testing strategy, 4 LUTs have been configured similarly. Consequently, the output values of all LUTs will be equal for each input vector. Then in 16 clock cycles (test time), TPG (up-counter) applies 0 to 15 to the LUTs' inputs. In each cycle, the output of 3 golden LUTs are compared using a 3-input XOR gate [26] and the output of first golden LUT and CUT (Circuit Under Test) are compared using a 2-input XOR gate. If all of LUTs are fault free then the outputs of XOR gates will be zero in test time. On the other hand, if i^{th} cell in one LUT becomes faulty, there will be at least one pulse at the i^{th} cycle in the output of XOR gates. To complete the diagnosing, we must have two configurations for ORA. In first configuration LUTs 2, 3 and 4 are considered as golden LUTs and LUT 1 is considered as CUT. In second configuration LUTs 1, 2 and 4 are golden LUTs and LUT 3 is CUT. Diagnosing of faulty LUT can be deduced using Table 1.

Table 1. Diagnosing faulty LUTs.

Faulty LUT	Configuration 1		Configuration 2	
	Among Goldens (2 & 3 & 4)	Between Golden & CUT (1 & 4)	Among Goldens (1 & 2 & 4)	Between Golden & CUT (1 & 3)
LUT1	pass	fail	fail	fail
LUT2	fail	pass	fail	pass
LUT3	fail	pass	pass	fail
LUT4	fail	fail	fail	pass
All LUTs	fail	fail	fail	fail
Not LUTs	pass	pass	pass	pass

For example, if LUT2 becomes faulty then the outputs of two XOR gates will be failed (contains a pulse at i^{th} clock cycle) and passed (without pulse) respectively in the first configuration and the similar results for second configuration will be occurred. After detection of faulty LUT using Table 1, we can locate the fault source according to the cycle time in which the pulse has been occurred. If the pulse be occurred in 13th clock cycle, then the faulty elements will belong to the 13th SRAM cell or the path from cell's output to the LUT's output (Figure 5).

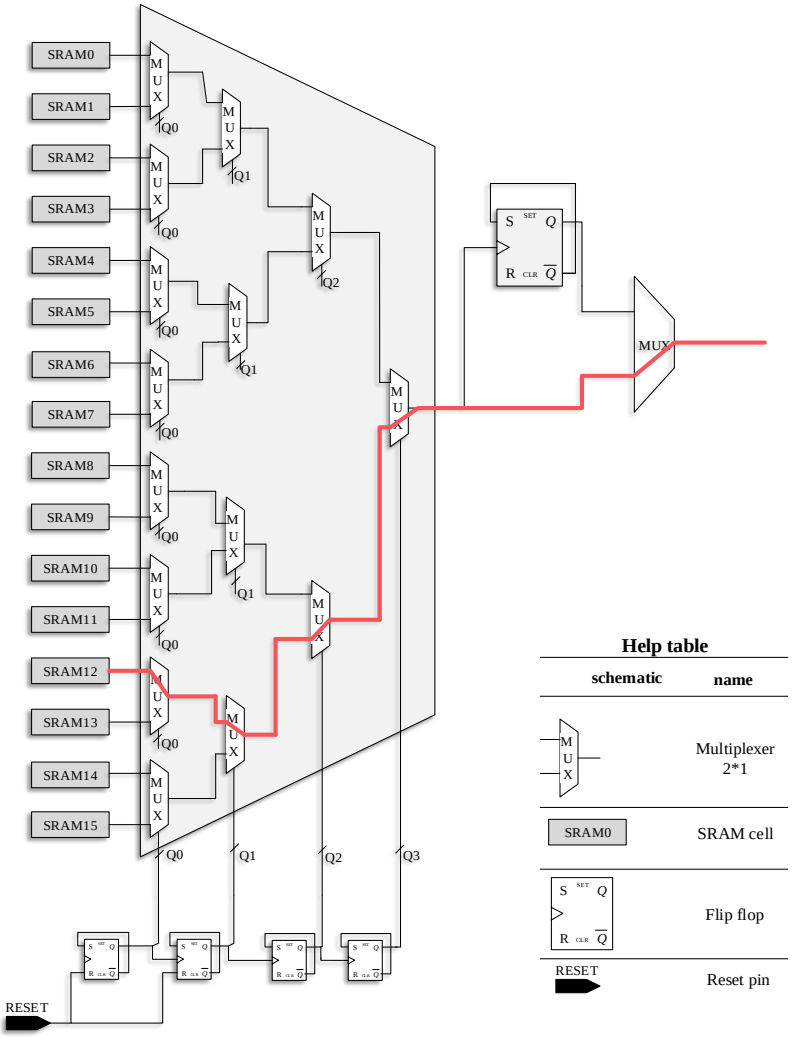

Figure5. SRAM cell and related path in diagnosing step.

A test input (T) is determined the test or normal mode operation of CLB. In normal mode the CLB primary inputs determine the inputs' logic values of LUTs and the BIST has no intervention in CLB operation. The modified CLB architecture (including BIST core) has been shown in Figure 6.

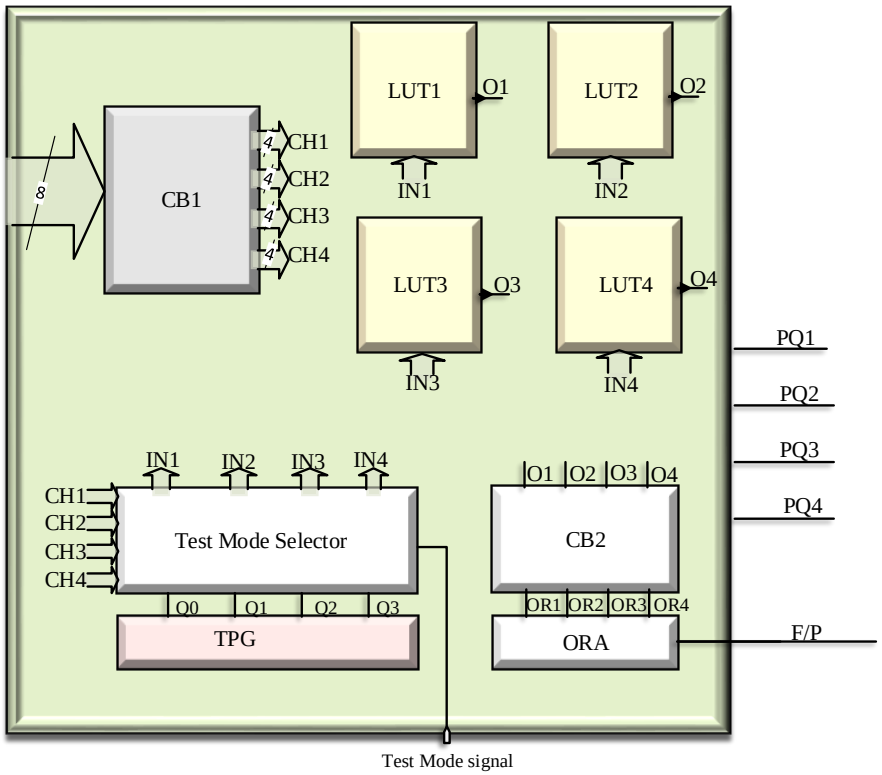

Figure 6. CLB architecture including BIST core.

There are 4 LBs in a CLB (LB1- LB4), each of them contains an LUT, a MUX 2×1 and a DFF. A CLB has 8 primary inputs (PIs) which can be connected to any LUTs' inputs through connection box 1 (CB1). The architecture of CB1 has been illustrated in Figure 7. Eight horizontal lines have been connected to PIs and the 16 vertical lines have been grouped in 4 channels each of them related to an LB's inputs. In an intersection point of horizontal and vertical lines of CB1 a programmable switch (PS) has been inserted. The ON/OFF state of the PSs has been determined in FPGA configuration step. For example, the blue PSs in Figure 7 are ON and the black PSs are OFF.

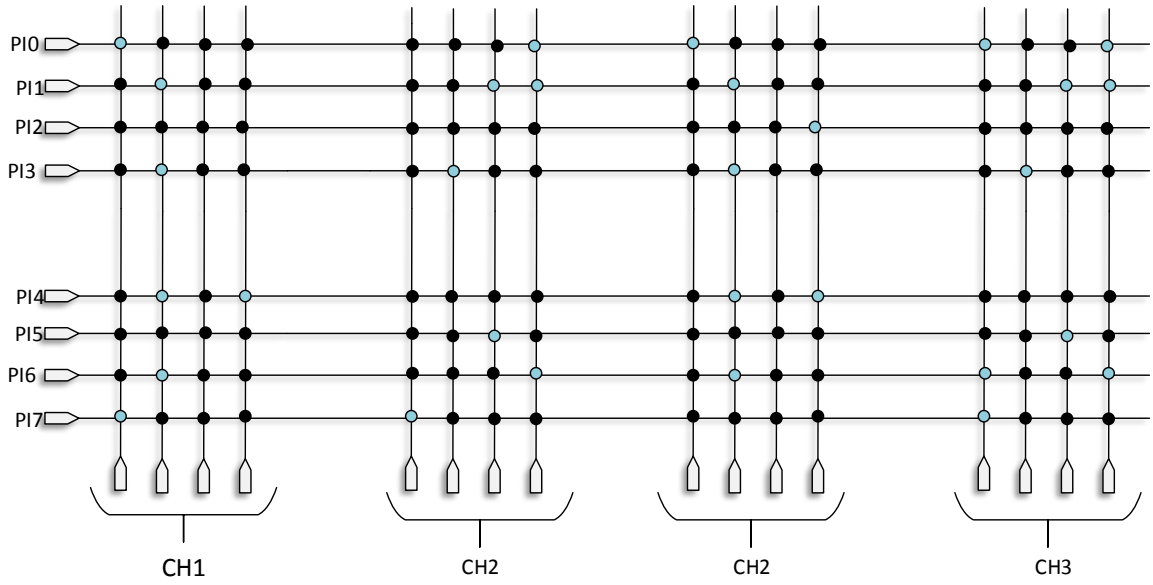

Figure 7. Connection box (CB1) internal architecture.

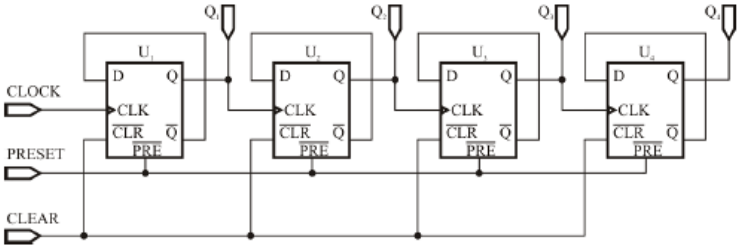

Figure 8. Proposed TPG.

In our test approach the TPG is a 4-bit up-counter [27] which has been shown in Figure 8. The synchronous reset line of this counter has been controlled by T input of CLB. When the CLB enters test mode this line has been assigned with 0 and the counter starts counting. In normal mode the reset line prevents the counter from counting. The output of TPG and the four channels of CB1 have been connected to the inputs of TMS module (Test Mode Selector). The internal circuit of this module has been illustrated in Figure 9.

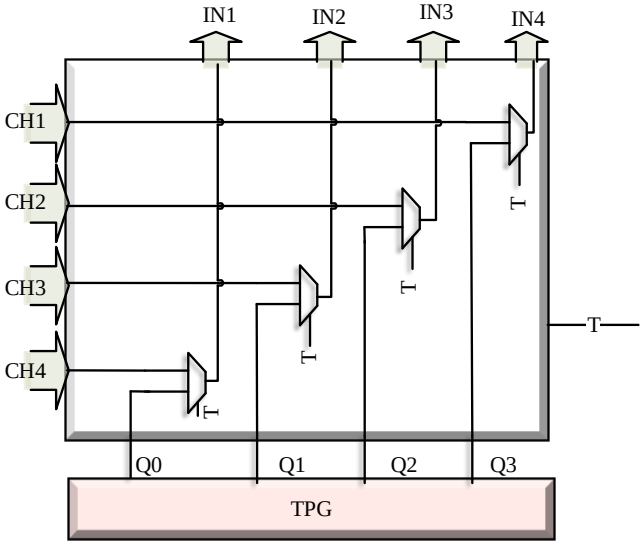

Figure 9. Test Mode Selector.

For each input group of LBs (IN1-IN4), there are four MUX 2×1s which select the corresponding lines of CB1's output channels (CH1-CH4) or one of TPG's outputs. For example, if the FPGA be in normal mode the first line of CH1 will be connected to first line of IN1, on the other hand if FPGA be in test mode the first line of TPG's output will be connected to the first line of IN1.

The ORA in proposed architecture consists of two XOR gates; a 3-input XOR gate compute the difference among the outputs of golden LUTs and a 2-input XOR gate to compute the difference between first golden LUT and the CUT (Figure 10).

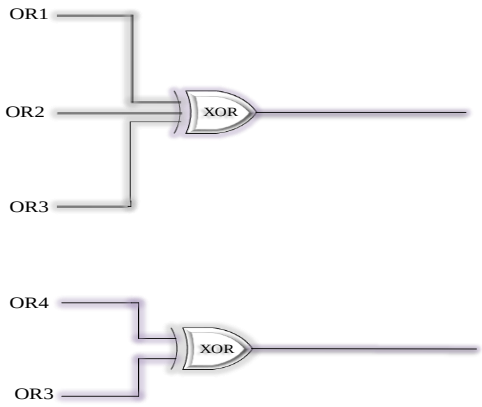

Figure 10. ORA circuitry.

As mentioned above in our test approach two configurations have been applied to diagnose the faulty LUT. For implementation of these two configurations we insert another connection box (CB2) in the input side of ORA. The internal architecture of CB2 has been shown in Figure 11. The outputs of LUTs have been connected to vertical lines of CB2 and the horizontal lines of CB2 have been connected to ORA's inputs (OR1-4). The ON/OFF states of CB2's PSs for two configurations have been illustrated in Figure 11.

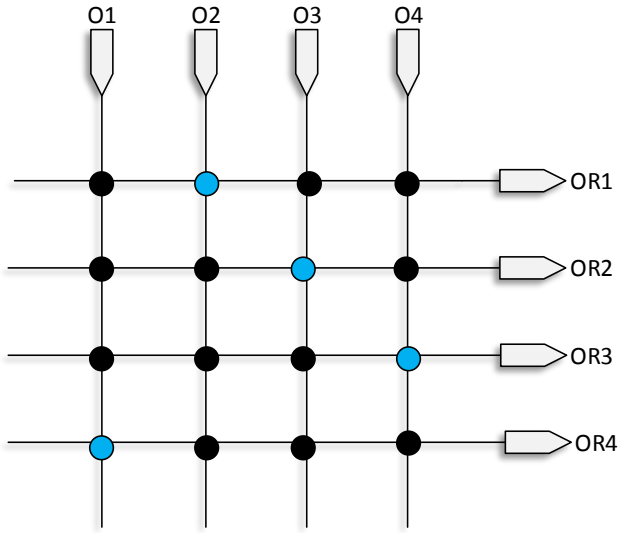

Figure 11. Connection box (CB2) internal architecture.

3- Simulation Results

In this section we briefly present the simulation results of proposed BIST method. All simulation results have been derived using HSPICE software. We have used the 45nm-PTM transistor model. In this experiment we have configured the LUTs using a random bit stream. We have assumed that 14th cell of LUT3 be stuck at 0. The resulted waveforms have been indicated in Figure 13.

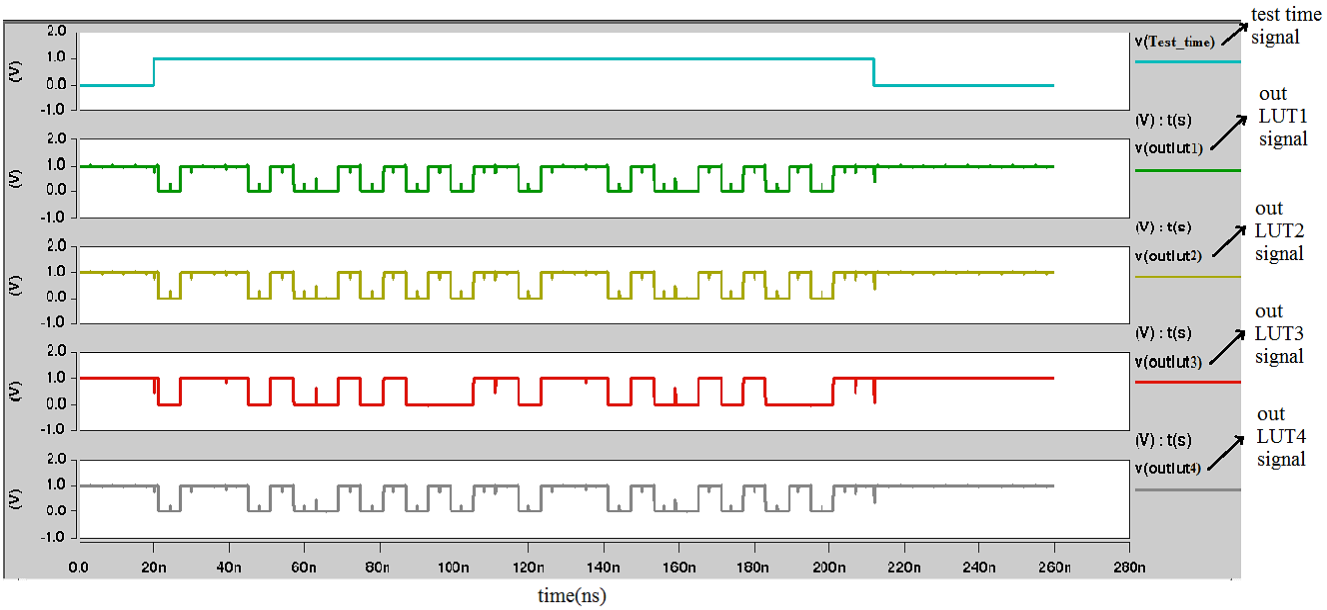

Figure12. Simulation results for single-cell fault in 3rd LUT.

The test signal (T) are high during test time (20 ns - 116 ns) and the outputs of TPG have been assigned to LUTs' inputs. The outputs of LUT1-4 have been indicated in this figure. As shown the output signals of LUT1,2 and 4 are similar but there is a missing high pulse at 14th clock cycle of LUT3's waveform. In Figure 14 the outputs of XOR gates in first configuration have been illustrated. In the 14th clock, the output of 3-input XOR has been failed and the output of 2-XOR gate is passed. The same signals have been indicated in Figure 15 for second configuration. In this figure at 14th clock cycle the output of 3-input XOR is passed and the output of 2-input XOR gate has been failed.

According to Table 1 outputs are matched with third column which indicates the 3rd LUT be faulty.

The area overhead of the proposed BIST-based approach has been computed using transistor counting. In our implementation of conventional and BIST-included CLBs number of transistors are 896 and 1072 respectively. So the area overhead will be 19% for proposed method. In another simulation we have compared the amount of leakage power in conventional and BIST included CLBs which indicated approximately 25% increase in proposed architecture.

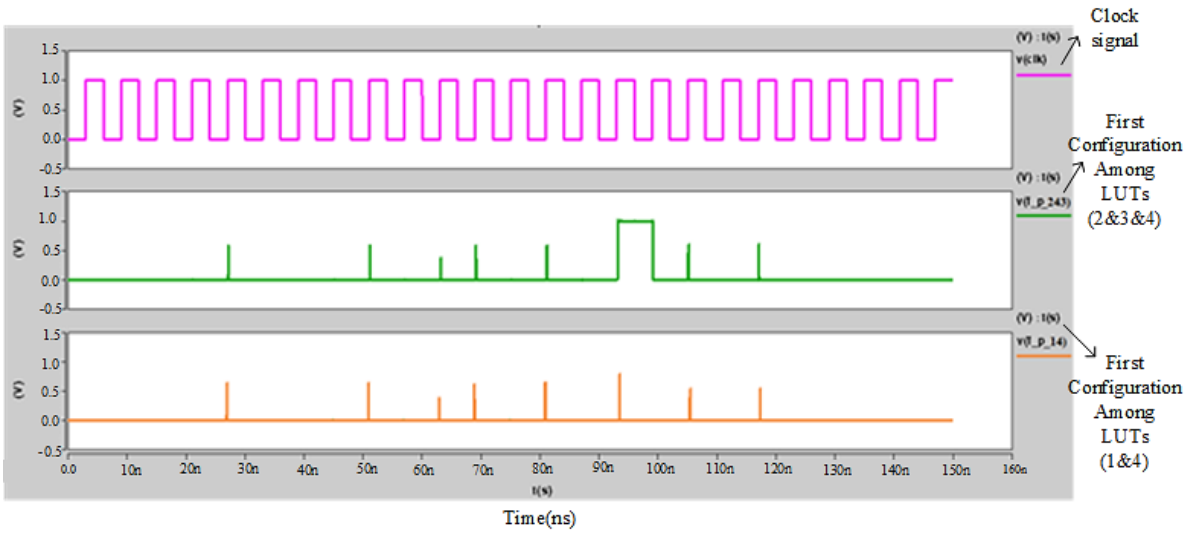

Figure13. ORA outputs for 13th cell be faulty in 3rd LUT in configuration 1.

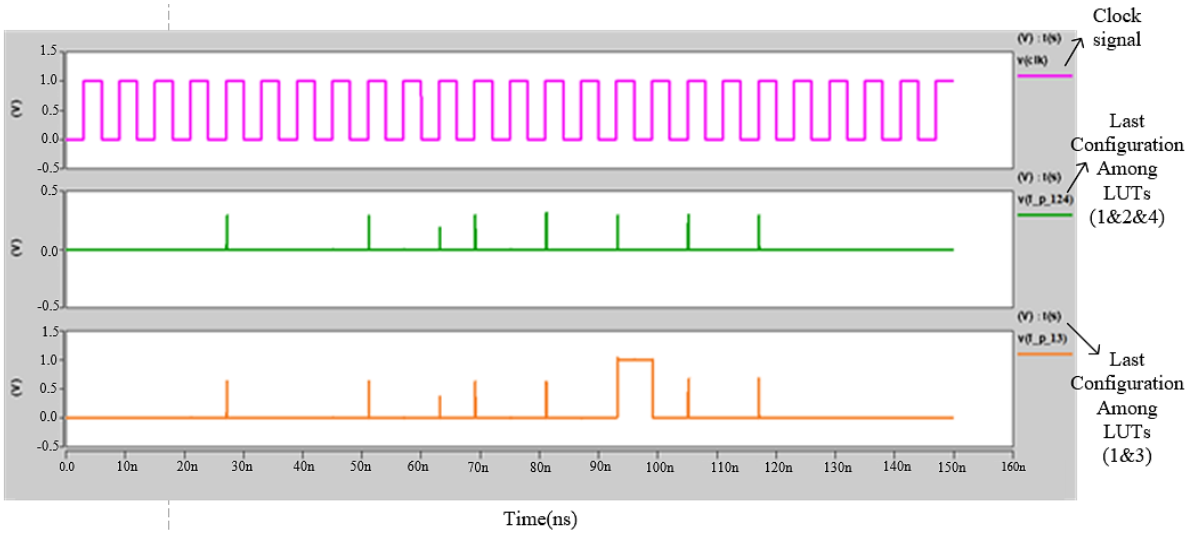

Figure14. ORA outputs for 13th cell be faulty in 3rd LUT in configuration 2.

4- Conclusion

Using BIST technique in circuit test has more advantages compared to normal counterpart. Automatic test equipment ATE for constructing normal test in conventional VLSI circuits includes hardware test using expensive hardware and long solution. This makes the test complicated and high cost is spent on tester at each second. Most complicated test equipment cannot be used for higher level tests. Therefore, BIST logic structure is designed for VLSI circuits which can be useful for other test purposes like repair and maintenance, detection or driving test.

FPGA chips are playing a great role in current digital systems. According to their importance and by increasing the number of faults in such chips, developing efficient test methods is necessary. In this paper BIST-based architecture has been proposed to detect any single stuck-at faults in the LUTs of each CLB. We use 4-bit counter to produce exhaustive test vectors and a combination of XOR gates for ORA. Simulation of proposed architecture in HSPICE has shown 100% fault coverage along with 19% area and 25% leakage power overheads.

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