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A Novel Fully Differential Second Generation Current Conveyor and Its Application as a Very High CMRR Instrumentation Amplifier

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Abstract

This paper aims to introduce a novel Fully Differential second generation Current Conveyor (FDCCII) and its application to design a novel Low Power (LP), very high CMRR, and wide bandwidth (BW) Current Mode Instrumentation Amplifier (CMIA). In the proposed application, CMRR, as the most important feature, has been greatly improved by using both common mode feed forward (CMFF) and common mode feedback (CMFB) techniques, which are verified by a perfect circuit analysis. As another unique quality, it neither needs well-matched active blocks nor matched resistors but inherently improves CMRR, BW, and power consumption hence gains an excellent matchless choice for integration. The FDCCII has been designed using 0.18 um TSMC CMOS Technology with ±1.2 V supply voltages. The simulation of the proposed FDCCII and CMIA have been done in HSPICE LEVEL 49. Simulation results for the proposed CMIA are as follow: Voltage CMRR of 216 dB, voltage CMRR BW of 300 Hz. Intrinsic resistance of X-terminals is only 45 Ω and the power dissipation is 383.4 µW. Most favourably, it shows a constant differential voltage gain BW of 18.1 MHz for variable gains (here ranging from 0 dB to 45.7 dB for example) removing the bottleneck of constant gain-BW product of Voltage mode circuits.

Keywords:

Current-mode;
Instrumentation Amplifier;
CMIA;
FDCCII;
Very High CMRR.

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1- Introduction

In the last decades, researchers and designers of analog processors have been faced with serious challenges in the design of low-voltage (LV), low-power (LP) circuits and systems. That is due the increasing demand for mobile and battery powered equipment and also technology down scaling trend [1]. Current mode (CM) signal processing/design as a promising solution to these challenges has thus gained more popularity [1-5]. As the main reason of the superiority of CM processors over the Voltage Mode (VM) ones can name: the wider dynamic range, simpler circuitry, wider BW, higher speed/frequency, lower supply voltage and consumed power [4-14]. Besides, while the Voltage Mode Instrumentation Amplifiers (VMIA) seriously suffer from problems of dependency of BW on gain and CMRR value, and need tightly matched resistor (to improve the CMRR), most favorably, the Current Mode Instrumentation Amplifiers (CMIA) are free from such requirements [6-18]. Various structures of CMIA have yet been reported, among which CMIAs based on FDCCIIs take the lead; because these structures are free from well-matched active blocks, as well as matched resistors to gain a high CMRR. The second generation current conveyors (CCIIs) are active blocks that have been used in many analog circuits such as oscillators [19-23], active filters [24-26] and amplifiers [6-18] to grant current mode benefits. The fully differential type of CCIIs [19-22] benefits from differential input and output terminals that are strongly acknowledged today. In this paper we seek to design a novel FDCCII structure to realize a high CMRR IA.

2- Proposed FDCCII

Functional block diagram and operational matrix of an ideal FDCCII are shown in Figure 1 and Equation 1, respectively.

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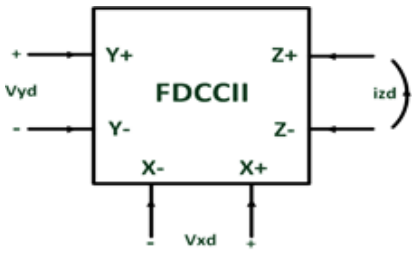

Figure 1. Block diagram of FDCCII.

$$\begin{bmatrix} i_{y+} \\ i_{y-} \\ v_{x+} \\ v_{x-} \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{y+} \\ v_{y-} \\ i_{x+} \\ i_{x-} \\ v_{z+} \\ v_{z-} \end{bmatrix} \quad (1)$$

Given Figure 1 and Equation 1, ideal FDCCIIs are current mode building blocks with six terminals that named as Y_+, Y_-, X_+, X_- , Z_+ and Z_- . Ideally the differential voltage of the X-terminals, V_{xd}, follows the differential voltage of the Y-terminals, V_{yd}, and the differential current of the Z-terminals, i_{zd}, follows the differential current of the X-terminals, i_{xd}. It means that ideal input impedance of Y-terminals, input (output) impedance of X-terminals and output impedance of Z-terminals are infinite, zero, and infinite, respectively. In real conditions, undesirable effects in FDCCII's function results from the non-ideal impedances in these terminals.

The CMOS transistor level realization of the proposed FDCCII is shown in Figure 2. Since this FDCCII has been intended for applications of instrumentation amplifier, thus, the design has been focused to improve its voltage CMRR. Like the most of already reported FDCCIIs, the voltage following operation of this FDCCII depends on the equalizing rate of output currents of two included transconductors. Practically, transistors M1-M2 and M5-M6 as the differential pairs of input stage transconductors must be tightly matched for a unity differential voltage gain from Y to X terminal. This differential pairs share the active loads M25-M26.

The transistors M4, M7 have been employed to fix common mode voltage of nodes B and C by using CMFF technique resulting in voltage CMRR improvement (by the factor of ε_4, as is explained in section 3). Actually these pairs, in addition to current mirror M24-M26, generate currents equal to common mode currents of M2 and M5 result in fix common mode voltages of nodes B and C. Moreover, the transistors M3 and M8 have been employed to fix common mode voltages of nodes (X_+, X_-) and (B, C) by using CMFB technique results in voltage CMRR improvement. Any common mode voltage at X-terminals causes common mode currents in M3 and M8 that along with current mirror M24-M26 generate the same currents in transistors M25-M26 resulting in fixated common mode voltages at nodes (X_+, X_-) and (B,C) (by the factor of ε_4, as is explained in section 3). To prevent the common mode voltage amplifying in drains of M11 (dM11) and M12 (dM12) (by the factor of $\varepsilon_5+\varepsilon_6$, as is explained in section 3), a CMFF technique has been employed as the pair of M29-M30 and current mirrors of M11-M13 as follows: The pair of M29-M30 apply a current equal to the common mode current of M27 and M28 to current mirror M11-M13, then there is no common mode current passing through impedances of nodes dM11 and dM12. Transistors M21-M22 that must be matched for symmetry, are the voltage buffer stages. Two identical class-A output stages consisting of M33 and M34 are the current buffer stages. These stages mirror X-terminals differential current to Z-terminals and for a unity differential current gain must be matched with corresponding transistors of the X-terminals branches (M31-M32). In the current following action of the output stages, simple current mirror M18-M20 along with transistors M35-M36 remove common mode currents passing through Z-terminals (by the factor of $\varepsilon_2+\varepsilon_3-\varepsilon_1$ as is explained in section 3) using the same CMFF technique as the one is already explained.

Driving the mentioned current buffer and voltage buffer blocks (see Figure 2) are determined by v_{ocm} which is generated by the CMFB block consisting of current mirror M16-M17 and differential pair of M37-M38 (see Figure 2).

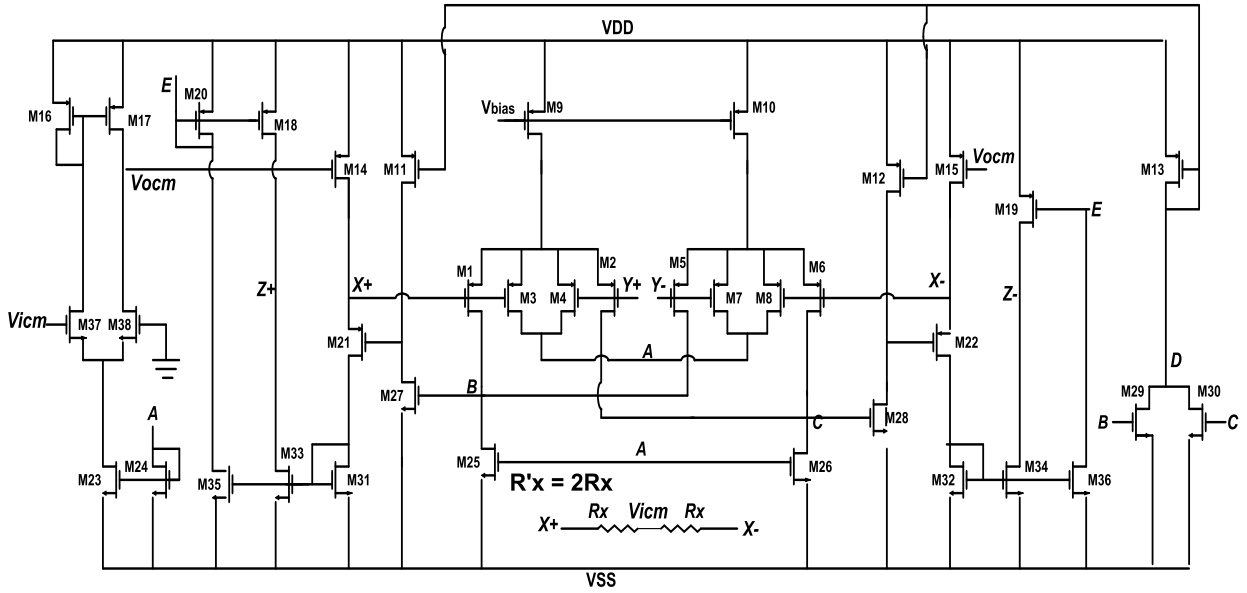

Figure 2. Transistor level structure for proposed FDCCII.

Function of the CMFB block is to fix common mode voltage of X-terminals to zero using negative feedback structure. By applying common mode voltage to Y-terminals, the common mode voltage of X-terminals is increased which flows a common mode current in the external resistance of Rx and increasing the common mode voltage in node V_{icm}. This increased voltage stimulates differential pair of M37-M38 to increase V_{ocm}, resulting in identical common mode currents in M14-M15. Finally, this negative feedback prevents the passing of input common mode current through M21-M22 resulting in great improvement of CMRR. It is worth mentioning that in this work, R' x is an external resistor placed between X terminals (that is shown as two series resistors of Rx in Figure 2) to form the suitable X inputs and Z outputs currents, thus should sufficiently be larger than internal resistance of X-terminals (r_x).

3- Circuit Equations

In this section, a full small signal analysis of the circuit performance is expressed. All transistors of the novel FDCCII are assumed to be operating in saturation region. It should be noticed that transistors M11-M12, M14-M15, M18-M19 and M25-M26 function as constant and variable current sources respectively for differential and common mode inputs. This is because of parallel connected pairs of M3-M4, M7-M8, M29-M30, M35-M36 (which don't respond to differential inputs) and V_{icm} which is zero for differential inputs.

If differential voltage of $Y_+ - Y_- = V_d$ ($Y_+ = -Y_- = V_d/2$) is applied to Y-terminals, Equations 2 to 4 could be concluded for FDCCII circuit (in this case $g_{m5\text{-}8} = g_{m5}$ and $g_{m1\text{-}4} = g_{m1}$ and no R'_X between X-terminals are assumed):

$$V_{(B)} = -V_{(C)} = (i_{ac1} + i_{ac6})R_{outB} = -g_{m1}.R_{outB}\frac{Y_+ - Y_-}{2} - g_{m2}.R_{outB}\frac{X_- - X_+}{2} \quad (2)$$

$$V_{dM11} = -V_{dM12} = -i_{ac27}R_{outdM11} = -g_{m27}.R_{outdM11}.V_{(B)} \quad (3)$$

$$V_{xadiff} = -V_{xbdiff} = V_{dM11}.\frac{r_{o14}}{r_{o14} + \frac{1}{g_{m21}}} = -V_{dM12}.\frac{r_{o14}}{r_{o14} + \frac{1}{g_{m21}}} \quad (4)$$

Using Equations 2 to 4, differential voltage gain from Y-terminals to X-terminals (while there is no external resistor R'_X between X-terminals) can be found as Equation 5:

$$Av_{xdiff} = \frac{V_{xdiff}}{V_{indiff}} = \frac{g_{m1}.g_{m27}R_{outB}.R_{outC}\dfrac{r_{o14}}{r_{o14} + \frac{1}{g_{m21}}}}{1 + g_{m5}.g_{m27}R_{outB}.R_{outC}\dfrac{r_{o14}}{r_{o14} + \frac{1}{g_{m21}}}} \approx \frac{g_{m1}}{g_{m5}} \quad (5)$$

Assuming $g_{m1}=g_{m5}$, results a unity differential voltage gain from Y to X terminals. Using loop gain of differential negative feedback (c.f. denominator of Equation 5) assists to find X-terminals intrinsic floating resistance

$$r_x = \frac{2(r_{o14} // \frac{1}{g_{m21}})}{1 + g_{m5}.g_{m27}.R_{outB}.R_{outC}\frac{r_{o14}}{r_{o14} + \frac{1}{g_{m21}}}} \quad (6)$$

Because of unity differential current gain of the output stage, the differential voltage gain from Y-terminals to each one of Z-terminals (when there are external resistor of R'_X between X-terminals and external grounded loads of R_z at Z-terminals) could be expressed as Equation 7:

$$Av_{zdiff} \cong \frac{g_{m1}}{g_{m5}} . \frac{R_Z}{R'_X + r_x} \quad (7)$$

Assuming $g_{m1}=g_{m5}$ and a constant R'_X, the differential voltage gain of Av_{zdiff} of Equation 7 becomes mainly determined by the ratio of $R_{Z//}\, r_x$. Similarly, if common mode voltages of Y+ = Y- = V_{cm} are applied to the voltage inputs of the FDCCII, the small signal equations for conveying input signals to X-terminals can be expressed as follows (assuming, $g_{m1} = g_{m5}$):

$$V_{(B)} = V_{(C)} = (i_{1cm} + i_{5cm} - i_{25cm})R_{outB} = -\varepsilon_{c4}.R_{outB}.\frac{g_{m1}}{1 + 4g_{m1}.r_{o9}}(V_{incm} + V_{xcm}) \quad (8)$$

$$V_{dM11} = V_{dM12} = (i_{11cm} - i_{27cm})R_{outdM11} \cong (\varepsilon_{c5} + \varepsilon_{c6})R_{outdM11}.g_{m27}.V_{(B)} \quad (9)$$

$$V_{x+cm} = V_{dM11}\frac{g_{m21}\, g_{m31}}{g_{m31}(g_{m21} + r_{o21}) - \frac{g_{m31} + r_{o21}}{r_{o14} // R_x}} \quad (10)$$

From Equations 8 to 10, common mode voltage gain to X-terminals is as follows:

$$Av_{xcm} = \frac{V_{xcm}}{V_{incm}} = \frac{\varepsilon_{c4}(\varepsilon_{c5} + \varepsilon_{c6})\frac{g_{m21}\, g_{m31}}{g_{m31}(g_{m21} + r_{o21}) - \frac{g_{m31} + r_{o21}}{r_{o14} // R_x}}\frac{g_{m1}.g_{m27}R_{out(B).}R_{out(dM11)}}{1 + 4\, g_{m1}r_{o9}}}{1 - \varepsilon_{c4}(\varepsilon_{c5} + \varepsilon_{c6})\frac{g_{m21}\, g_{m31}}{g_{m31}(g_{m21} + r_{o21}) - \frac{g_{m31} + r_{o21}}{r_{o14} // R_x}}\frac{g_{m1}.g_{m27}R_{out(B).}R_{out(dM11)}}{1 + 4\, g_{m1}r_{o9}}} \quad (11)$$

Now the total common mode voltage gain from Y-terminals to Z-terminals (while there are external resistor of R'_X between X-terminals and external grounded loads of Rz at Z-terminals) can be concluded as Equation 11:

$$Av_{zcm} = \frac{iz_{cm}.R_z}{V_{incm}} \cong \frac{\varepsilon_{c4}(\varepsilon_{c5} + \varepsilon_{c6}) \times (\varepsilon_{c2} + \varepsilon_{c3} - \varepsilon_{c1})\, g_{m1}.\, g_{m21}.\, g_{m27}.R_{out(B).}R_{out(dM11).}R_z}{1 + 4\, g_{m1}r_{o9}} \quad (12)$$

Loop gain of feedback in the denominator of Equation 11 is very smaller than “one”, thus, can be ignored. Finally using Equations 6 and 12 gives voltage CMRR as Equation 13:

$$CMRR_V = \frac{Av_{zdiff}}{Av_{zcm}} \cong \frac{1 + 4\, g_{m1}r_{o9}}{\varepsilon_{c4}(\varepsilon_{c5} + \varepsilon_{c6}) \times (\varepsilon_{c2} + \varepsilon_{c3} - \varepsilon_{c1})\, g_{m5}.\, g_{m21}.\, g_{m27}.R_{out(B).}R_{out(dM11)}(R_x + r_x)} \quad (13)$$

Transistors dimensions of the proposed FDCCII is shown in Table 1. The dimensions have been optimized for loads of $R_{z+} = R_{z-} = R_L$=1 kΩ.

Table 1. Dimension of the transistors of the proposed FDCCII.

Transistors	W/L (µm/µm)
M1-M8	6 / 0.45
M9-M10	24.8 / 0.8
M11-M13	1.26 / 0.45
M14-M15	5 / 0.5
M16-M17	8 / 1.7
M18-M19	0.47 / 0.6
M20	0.47 / 0.9
M21-M22	13.5 / 0.7

M23, M25-M26, M27-M28	6.48 / 1.53
M24	12.96 / 1.53
M29-M30	3.24 / 1.53
M31-M34	0.77 / 1.9
M35-M36	0.3 / 2
M37-M38	1.17 0.9

4- Proposed CMIA and Simulation Results

The novel FDCCII has been improved specifically towards the application of instrumentation amplifier. Thus it can be used alone as an IA when both of its Z-terminals are connected to a grounded load resistor R_L. Configurations of the proposed CMIA for voltage input case is shown in Figure 3.

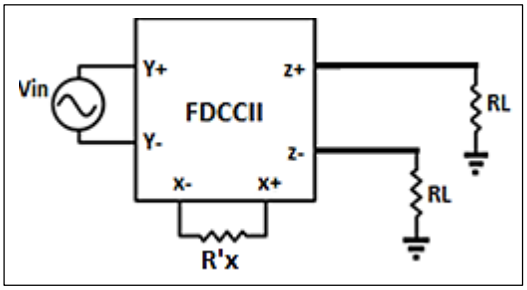

Figure 3. CMIA configuration for voltage inputs.

The most important specifications of the proposed circuit have been evaluated using HSPICE LEVEL 49 in 0.18 um TSMC CMOS Technology. It should be noticed that R'_X = 0.44 kΩ and V_{bias} = 600 mV (bias voltage connected to gate of M9 in Figure 2) has been used in the simulations. The results of the frequency response simulation at the several gains are shown in Figure 4 for voltage input case. Different gains are obtained (from 0 dB to 45.7 dB) using different values of the load resistors R_L (R_L =*0.44K*Ω-*150K*Ω). It can be seen that the BW is constant as 18.1MHz for different gains (the amount of R_L to maintain the same BW for differential voltage gain is limited to 150 *K*Ω). Favorably, Figure 4 shows that in the designed FDCCII there is no dependency between BW and gain, which exists in Voltage Mode (VM) circuits; the variation in the RL that results in the same variation in the voltage gain has no effect on the BW. The frequency responses of the voltage CMRR is shown in Figure 5. As it can be seen in Figure 5, the proposed CMIA has a CMRR of 216 dB with -3 dB BW of 300 Hz; with R_L=1 *K*Ω, R'_X=0.44KΩ.

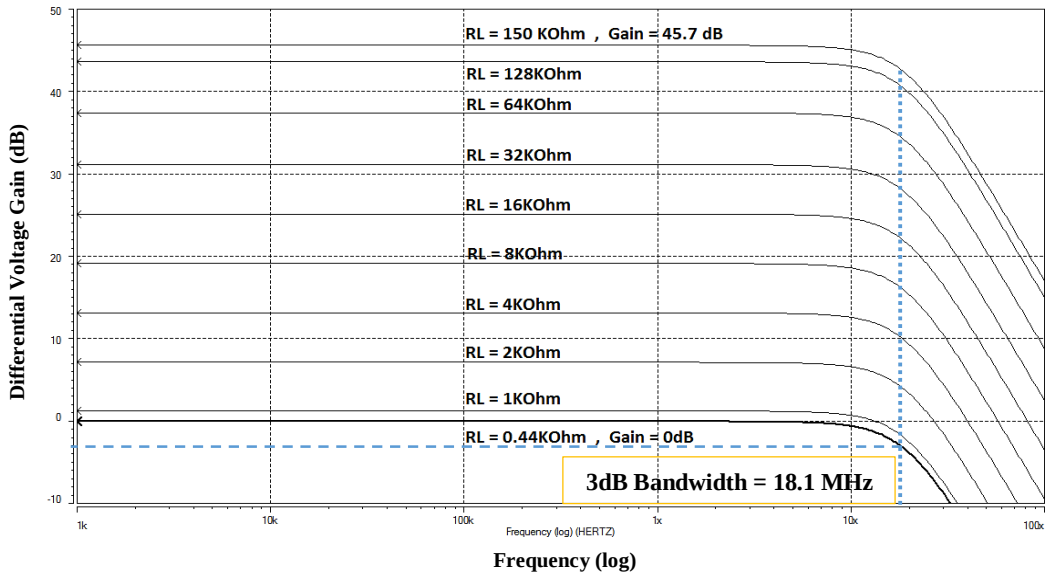

Figure 4. Frequency response of the voltage differential gains for different values of RL (.44KΩ-150KΩ).

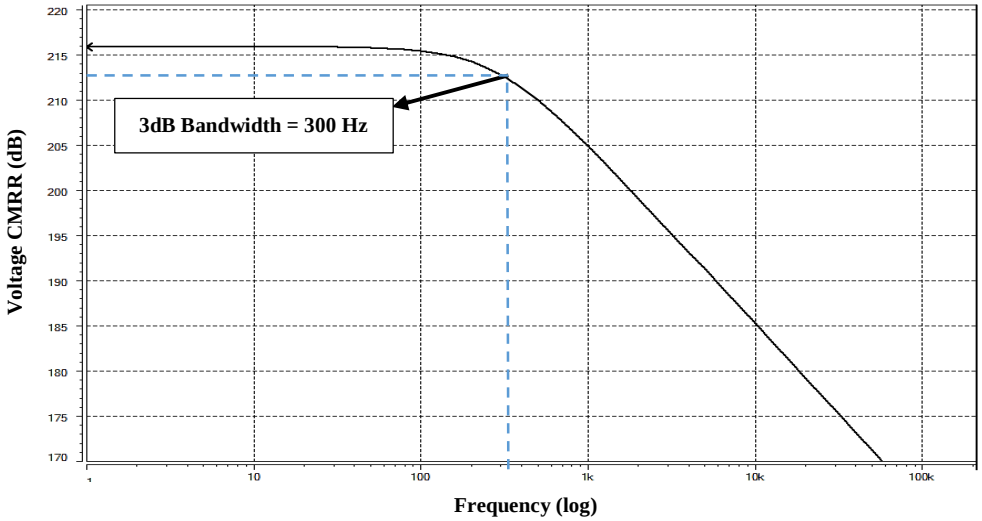

Figure 5. Voltage CMRR for proposed CMIA with RL=1 KΩ, R'_X=0.44KΩ.

Table 2 summarizes the performance simulation results of the proposed CMIA. Differential voltage gain varies from 0dB (R_L=0.44KΩ) to 45.7dB (R_L=150KΩ). Power consumption under ±1.2V supply voltage is only 383.4 µW, and X-terminals intrinsic floating resistance (r_x) is 45 Ω. The performance comparison between the proposed CMIA and some other artworks is summarized in Table 3.

Table 2. CMIA's performance specifications.

Voltage CMRR	216 dB
CMRR 3dB Bandwidth	300 Hz
Differential Voltage Gain Bandwidth (R_L≤150KΩ)	18.1MHz
Differential Voltage Gain(0.44KΩ ≤R_L≤ 150KΩ)	0 dB - to – 45.7 dB
Differential Voltage Gain Bandwidth product(MHz)	$18.1 * 10^6$ -to- $3.49 * 10^9$
Power Dissipation	383.4 µW
Supply Voltages	±1.2V
X-terminals intrinsic floating resistance (r_x)	45 Ω

As it can be seen in Table 3, the proposed CMIA exhibits superior performance in terms of CMRR value and differential gain BW for voltage input, very low (r_x) and low consumed power. Also, it doesn't need matched blocks.

Table 3. Comparison between the proposed CMIA and some other works

Specification	**[18]**	**[17]**	**[17]**	**[8]**	**[11]**	**[13]**	**Proposed**
Input Signal	Voltage	Voltage	Voltage	Voltage	Voltage	Current	Voltage
Technology	65 nm CMOS	130 nm CMOS	90 nm CMOS	0.18um CMOS	0.35um CMOS	0.18um CMOS	0.18 um CMOS
CMRR	88 dB[v]	64.7 dB[v]	76 dB[v]	110 dB[v]	107 dB[v]	91 dB[c]	216 dB
CMRR Bandwidth	< 6 KHz	100 KHz	14 KHz	NA[e]	NA[e]	1.15 kHz[c]	300 Hz
Differential Voltage Gain	<39 dB	< 61 dB	< 50 dB	0 dB	0 dB	0 dB	0 dB -to- 45.7dB
Differential Gain BW product	NA[e]	< 381 MHz	<56.9 MHz	NA[e]	8 MHz[v]	10.18 MHz[c]	18.1 MHz to 3.49 GHz
Power Dissipation	3.96 µW	14 µW	11 µW	420 µW	1.3 mW	219 ~ 446 µW	383.4 µW
Supply Voltages	1.2 V	0.4 V	0.4 V	±1.65 V	±1.5 V	±0.8 V	±1.2 V
Needs Matched Blocks	Yes	No	No	Yes	No	No	No

[c] for current input, [v] for voltage input, [e] not available

10- Conclusion

In this paper, a novel topology of a low power, very high CMRR, and wide BW CMIA is introduced. Its structure is based on one active block named FDCCII, which is designed based on novel structures and techniques, that eliminates the need for well-matched blocks to reach a very high CMRR for the proposed CMIA. The results of HSPICE simulations show that the CMRR value and BW as the most important properties of CMIAs, are greatly improved using CMFB and CMFF techniques. Because of its low power dissipation it can also be used for portable systems and well matched the down scale trend of the modern technologies.

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